Chapter 12
ISA BUS
PC Architecture for Technicians: Level-1

Systems Manufacturing Training and Employee Development

OBJECTIVES: At the end of this section, the student will be able to do the following:

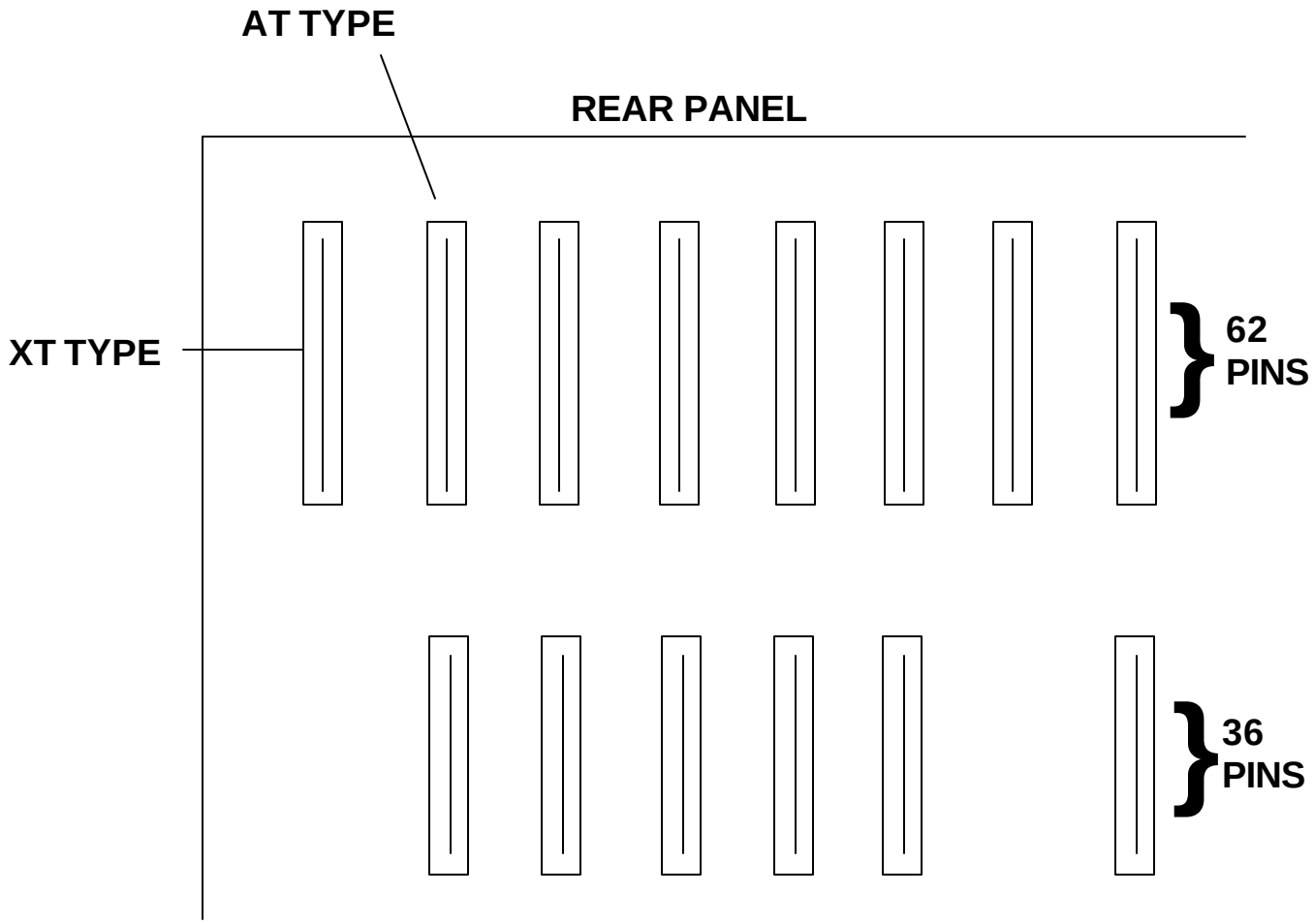
- Describe the background of the Industry Standard ISA Expansion Bus.
- Describe Typical System Bus Cycles.
- Explain the Functions of the Signals on the I/O Channel.
- Discuss the ISA BUS Signal Descriptions.
- Describe 8-bit Memory & I/O ISA BUS Cycles.
- Describe Conversion BUS Cycles.
- Describe 16-bit Memory & I/O ISA BUS Cycles.

ISA BUS OVERVIEW

ISA BUS OVERVIEW

- This chapter presents an overview of the ISA bus.
- The I/O channel (defined by IBM) is an expansion bus permitting the installation of a wide variety of adapter cards.
- The ISA bus is an industry-wide attempt to standardize the original IBM I/O Channel.
  - IBM did not fully document the PC/AT I/O Channel.
  - The IEEE approved an AT bus specification in 1987 which defined what is know as the Industry Standard Architecture bus, or ISA bus for short.
- The function of each ISA bus signal is presented and timing diagrams illustrate various ISA bus transfers.

IBM PC/AT System Board

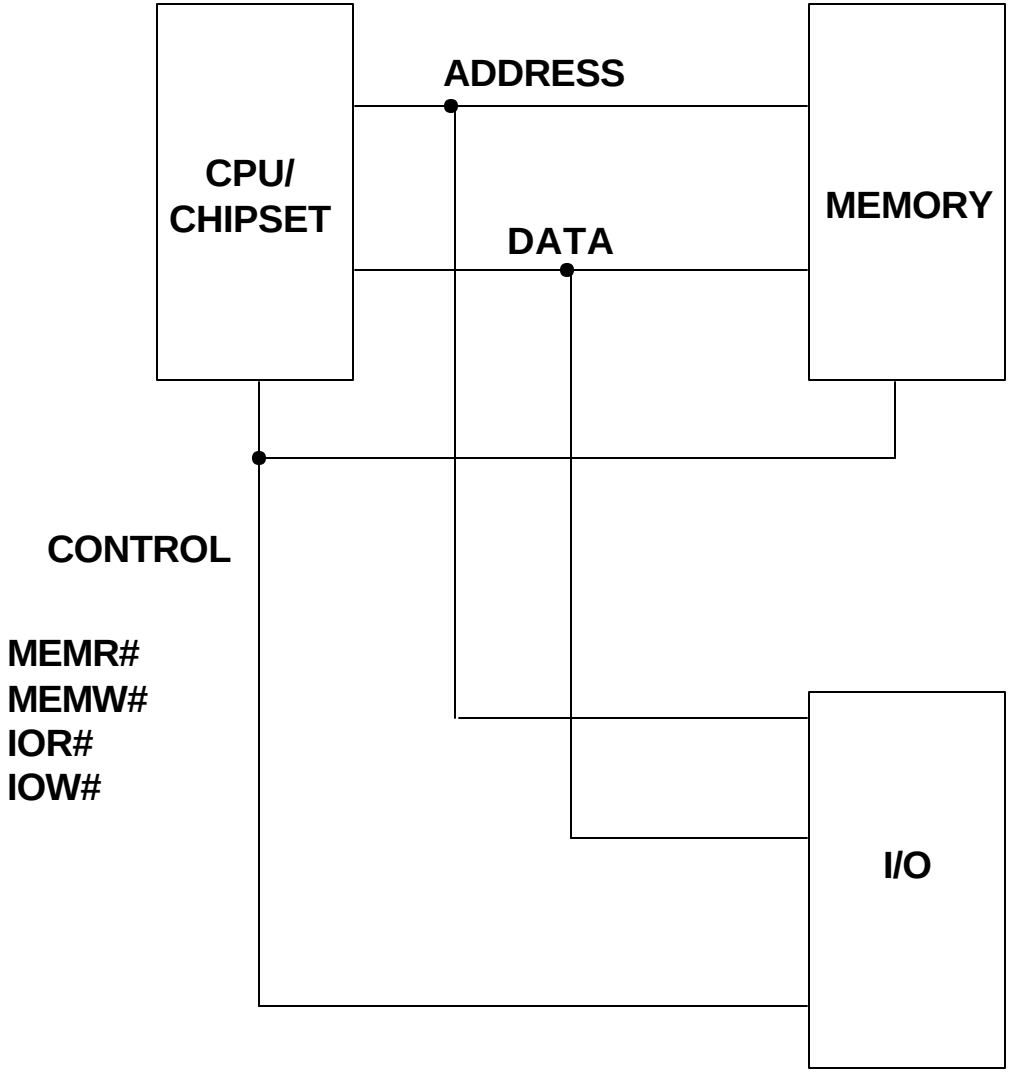


CURRENT ISA BUS STANDARD

- The I/O channel (8-bit) in the original PC and PC/XT consisted of several 62-pin connectors (slots).
- The ISA bus standard (IEEE P996) very closely matches the timing of the 8 MHz IBM PC/AT.
  - SYSCLK is is still 8 MHz but is no longer necessarily related to the CPU clock.
    - The CPU clock could be running at 25MHz, 33MHz, 50MHz, 60MHz, or 66MHz
    - SYSCLK is sometimes 8.33 MHz obtained from 25/3, etc.

TYPICAL SYSTEM BUS CYCLES

TYPICAL SYSTEM BUSES



TYPICAL SYSTEM BUSES

- **Recall that the typical microprocessor reads and writes to memory and I/O devices using the following three buses:**
- **ADDRESS BUS**
  - The address bus supplies an address to the memory or I/O device.
- **DATA BUS**
  - The data bus provides a bi-directional pathway for data flow. The data flow can be:
    - From the CPU to memory or I/O devices (WRITE).
    - From the memory or I/O devices to the CPU (READ).

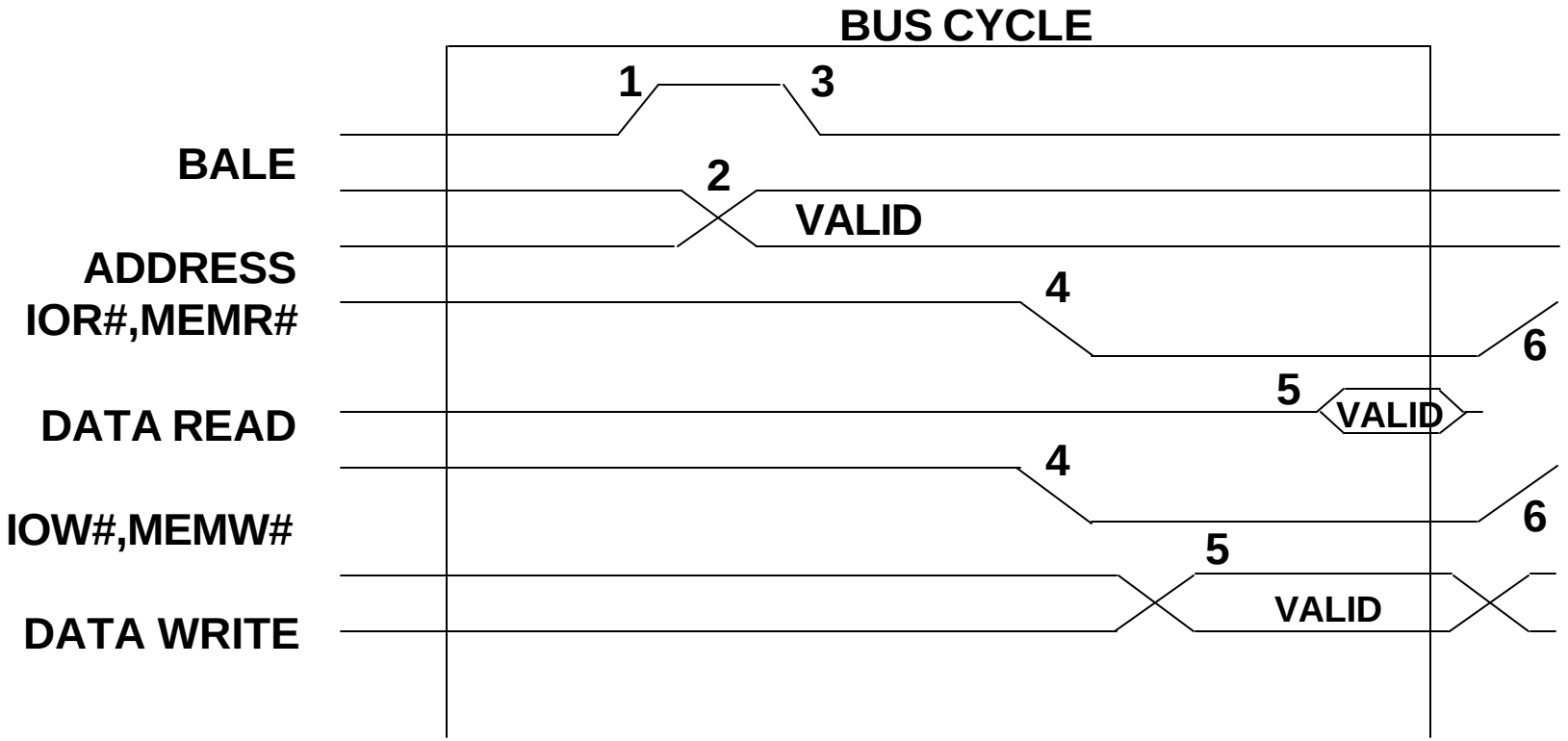
TYPICAL SYSTEM BUSES

CONTROL BUS

- The control bus provides the **control signals** (**commands**) that tell the memory and I/O devices what type of cycle the CPU is running. Typical commands follow:
- **MEMR#**
  - CPU READ FROM MEMORY
- **MEMW#**
  - CPU WRITE TO MEMORY
- **IOR#**
  - CPU READ FROM I/O DEVICE
- **IOW#**
  - CPU WRITE TO I/O DEVICE

Typical System Bus Cycle

The figure shows both a read and a write cycle. The timing of the bus signals in a typical bus cycle follows the steps on the next pages.



TYPICAL SYSTEM BUS CYCLE

CPU READ FROM MEMORY OR I/O DEVICE

1. BALE goes high, indicating the beginning of a bus cycle.
2. The ADDRESS bus becomes valid.
3. The ADDRESS bus is latched as BALE goes low.
4. The appropriate Command (MEMR#, IOR#) becomes active low.
5. The addressed memory or I/O device places the data on the DATA bus.
6. The cycle ends when the CPU samples the DATA bus as COMMAND goes inactive high.

TYPICAL SYSTEM BUS CYCLE

CPU WRITE TO MEMORY OR I/O DEVICE

1. BALE goes high, indicating the beginning of a bus cycle.
2. The ADDRESS bus becomes valid.
3. The ADDRESS bus is latched as BALE goes low.
4. The appropriate Command (MEMW#, IOW#) becomes active low.
5. The CPU places the data on the DATA bus.
6. The cycle ends when the CPU samples the DATA bus as COMMAND goes inactive high.

ISA BUS BACKGROUND

ISA BUS BACKGROUND

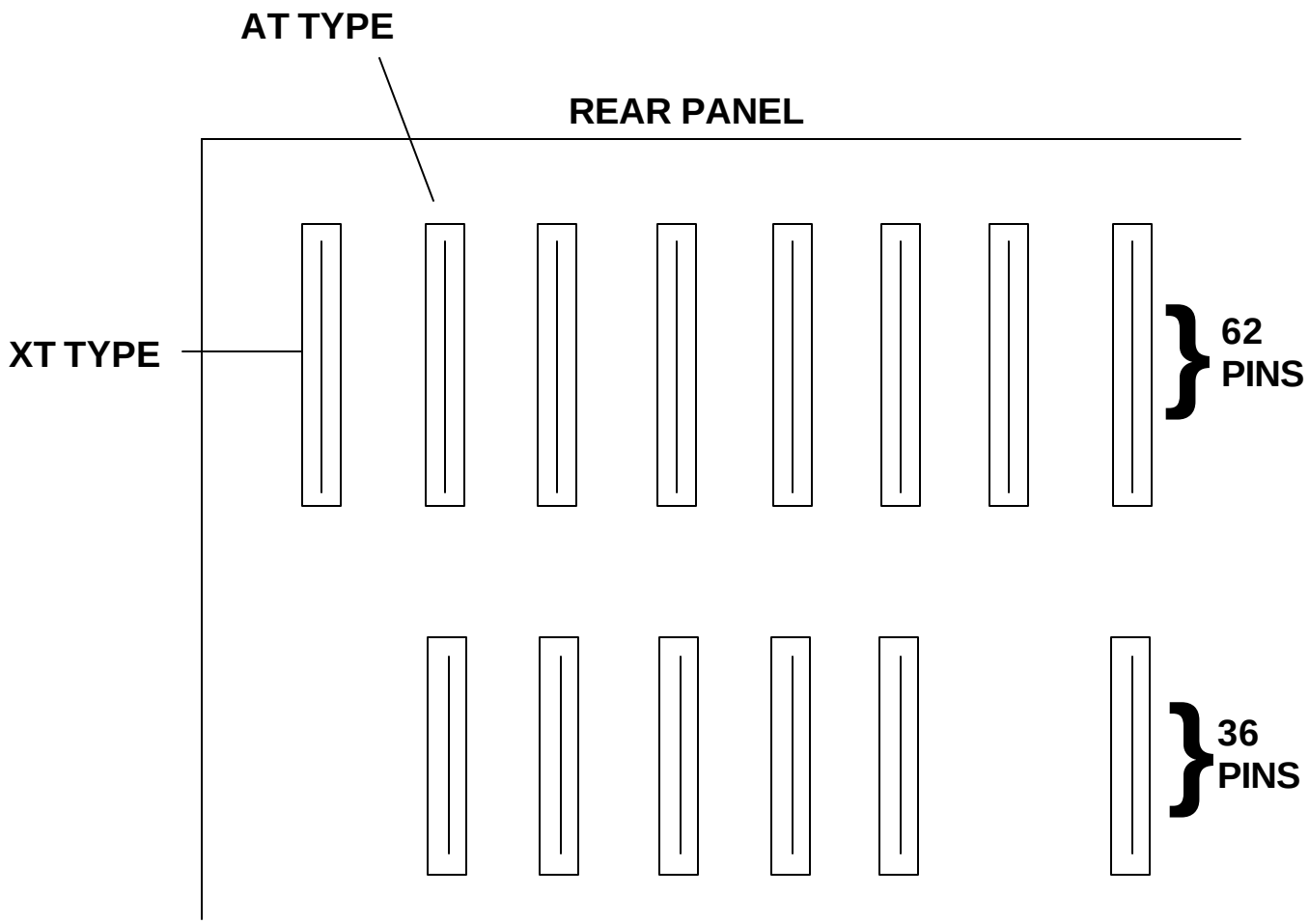
- The original PC 62-pin slot was not adequate for the PC/AT (80286 CPU) because of the need for the following:
  - more address lines--24 instead of 20
  - more data lines--16 instead of 8
  - more interrupts--5 interrupts added
  - more DMA--4 new DMA channels
  - various lines supporting 16-bit access

ISA BUS BACKGROUND

COMPATIBILITY WITH THE PC: To permit the PC/AT to accommodate the PC type of adapter cards, the 62-pin slot was left almost unchanged.

- A 36-pin extension was added to the original 62 pins to provide for the extra needs listed above.
  - The 36-pin extension is in line with the 62 pins,
    - Giving the PC/AT adapter card a 98-pin connection.
  - Most PC/ATs provide a mix of the old and new slots.
- The original IBM PC/AT had the following:
  - 6 of the **98-pin slots (62+36)**
  - 2 of the 62-pin slots

IBM PC/AT System Board



ISA 8-bit Connector Signals

ISA Bus 8-bit Connector

GND	B01	A01	**IOCHCK#**
RSTDEV	B02	A02	**SD7**
+5V	B03	A03	**SD6**
IRQ9/(IRQ2)	B04	A04	**SD5**
-5V	B05	A05	**SD4**
DRQ2	B06	A06	**SD3**
-12V	B07	A07	**SD2**
SRDY# (NOWS#)	B08	A08	**SD1**
+12V	B09	A09	**SD0**
0V	B10	A10	**IOCHRDY**
SMEMW#	B11	A11	AEN
SMEMR#	B12	A12	**SA1**
IOR#	B13	A13	**SA1**
IOW#	B14	A14	**SA1**
DACK3#	B15	A15	**SA1**
DRQ3	B16	A16	**SA1**
DACK1#	B17	A17	**SA1**
DRQ1	B18	A18	**SA1**
REFRESH#	B19	A19	**SA1**
SYSCLK	B20	A20	**SA1**
IRQ7	B21	A21	**SA1**
IRQ6	B22	A22	**SA**
IRQ5	B23	A23	**SA**
IRQ4	B24	A24	**SA**
IRQ3	B25	A25	**SA**
DACK2#	B26	A26	**SA**
TC	B27	A27	**SA**
BALE	B28	A28	**SA**
+5V	B29	A29	**SA2**
OSC	B30	A30	**SA**
GND	B31	A31	**SA**
			0

ISA 8-bit Connector Signals

The 62-Pin Portion of the ISA Bus Connector can be grouped into logical functions:

- **ADDRESS BUS (A19:0)**
  - These are OUTPUT ONLY signals used to address system-bus Memory & I/O
  - With 20 address lines (like the PC/XT), the system can address up to 1 MByte of Memory.
  - A19 is most significant bit , A0 is the least significant
- **DATA BUS (D7:0)**
  - These are Bi-directional data lines.
  - There are eight data lines (like the PC/XT).
  - D7 is most significant bit , D0 is the least significant.

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **CONTROL--The control bus consist of**:
  - Four **command** signals
    - **SMEMR#, SMEMW#, IOR#, IOW#**
  - & **IOCHRDY** (low to add wait states)
- **The fundamental purpose of the control bus is to identify the type of transaction and provide synchronization between the fast processor & the external devices it is reading from or writing to.**

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **CONTROL** (cont.)
  - **SMEMR#, SMEMW#:** System Memory Read/ Write Command
    - Indicates address bus contains a valid Memory Address.
    - Asserted for Memory Accesses below 1MB
  - **IOR#, IOW#: Input/Output Read/Write (IORC#, IOWC#)**
    - Indicates address bus contains a valid I/O Port Address.
  - **IOCHRDY: I/O Channel Ready (Active High)**
    - When IOCHRDY=1, the I/O Channel is READY.
    - Input only signal used to extend the ISA bus cycles for devices not fast enough to respond to normal cycles.
    - Pull Low to insert Wait States (I/O Channel NOT READY).

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **INTERRUPTS**--There are 6 interrupt request lines.
  - Input only lines used to generate Interrupt Requests to the system board 8259A PIC #1.
  - Note that IRQ9 was labelled IRQ2 on the PC/XT. The IRQ9 vector, type 71H, is redirected to the IRQ2 type 0AH to provide compatibility with XT type boards.
  - The interrupts are rising edge triggered.

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **DMA**--There are three DMA channels.
  - **Direct Memory Access Request/Acknowledge**
  - **DRQ**1-3--active high requests (8 bit)
  - **DACK**1# - DACK3#--active low acknowledge
  - TC--high pulse. NOTE: There is only one TC signal:
    - The DMA system supports a terminal count (TC) signal which indicates that one of the DMA channels is done.
  - Each DMA channel is capable of making a maximum of 64K, 8-bit transfers between memory and I/O devices

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **POWER:**
  - **+5V DC**
    - Used to power the logic on adapter cards.
  - **-5V DC- (Good signal to find pin B5 on ISA connector)**
    - Very little used. Originally supplied power to 16K-bit DRAM chips on older PCs.
  - **+12V DC**-
    - Used primarily for disk power, also for RS232.
  - **-12V DC**
    - Used for RS232.
  - **0V DC--GND (ground).**

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **CLOCKS**
  - **SYSCLK--System Clock (CLK, BCLK)**
    - This is typically 8 MHz.
    - It was originally the CPU clock on the PC/AT, first running at 6 MHz, then 8 MHz.
    - In modern PC's CLK will be about 8 MHz, not necessarily related to the CPU clock.
  - **84OSC--Oscillator Output (OSC) - 14.31818 MHz**
    - It is still used for clocking the 8254 Timer in the PC/AT.
      - 14.3MHz/12 = 1.19 MHz
    - Source of the CPU clock in the original PC (4.77 MHz).

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **ODDS AND ENDS**
  - **IOCHCK# -- I/O Channel Check (IOCHK#, CHCHK#)**
    - This active low signal is to provide adapter cards with a method of indicating memory failure.
    - It actually connects through gates to NMI and so is really non-maskable interrupt, type 2.(Active low).
  - **RSTDEV -- Reset Device (RESET, RSTDRV)**
    - This signal is active high **during power-on** to allow a reset of devices on adapter cards.

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **ODDS AND ENDS**
  - **BALE -- Bus Address Latch Enable (BUSALE, ALE)**
    - Active high during the beginning of a bus cycle. Addresses are latched on the falling edge.
    - BUSALE is held high during DMA transfers.
  - **AEN -- Address enable**.
    - A high indicates that the DMA system is in control of the bus
    - Used on the System Board to indicate that this is a NON CPU driven cycle.
      - Disables address decoders on System Board.

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **ODDS AND ENDS**
  - **SRDY# -- Synchronous Ready (OWS, NOWS)**
    - This signal, **Zero-Wait-State**, allows adapter cards to eliminate wait states on 16-bit memory cycles
    - Minimize wait states to two on 8-bit memory cycles.
    - This signal is active low and should be driven by the adapter card with an open-collector output device.
    - This is not available for I/O cycles.

ISA 8-bit Connector Signals (Cont.)

ISA Conn. 62-Pin Portion: Logical Functions (cont.)

- **ODDS AND ENDS**
  - **REFRESH# -- (MEMREF#)**
    - An active low signal indicating that a memory refresh cycle is in progress by the System Board.
    - Note, this signal becomes an input signal when another master is in charge of the bus. The other master can force the system board to run a refresh cycle. Must be done every 15.6 microseconds.

ISA 16-bit Connector Signals

ISA 16-bit Connector Signals

The 36-Pin Portion of the ISA Bus Connector

- **When the PC grew into the PC/AT, the need for more bus signals grew.**
- The original PC 62-pin slot was not adequate for the PC/AT (80286 CPU) because of the need for the following:
  - **More address lines -- 24 instead of 20**
  - **More data lines -- 16 instead of 8**
  - **More interrupts -- 5 interrupts added**
  - **More DMA -- 4 new DMA channels**
  - **Various lines supporting 16-bit accesses**

ISA Bus 16-bit Connector

MCS16#	D01	C01	SBHE#
IOCS16#	D02	C02	LA23
IRQ10	D03	C03	LA22
IRQ11	D04	C04	LA21
IRQ12	D05	C05	LA20
IRQ15	D06	C06	LA19
IRQ14	D07	C07	LA18
DACK0#	D08	C08	LA17
DRQ0	D09	C09	MEMR#
DACK5#	D10	C10	MEMW#
DRQ5	D11	C11	**SD8**
DACK6#	D12	C12	**SD9**
DRQ6	D13	C13	**SD10**
DACK7#	D14	C14	**SD11**
DRQ7	D15	C15	**SD12**
+5V	D16	C16	**SD13**
MASTER16#	D17	C17	**SD14**
GND	D18	C18	**SD15**

ISA 16-bit Connector Signals (Cont.)

The 36-Pin Portion of the ISA Bus Connector can be grouped into logical functions:

- **ADDRESS BUS (LA17-LA23)**
  - These Large Addresses, unlike the A0-A19 signals on the 62-pin connector, are **valid slightly earlier** (as much as 70ns) and are **NOT LATCHED**.
  - They are typically used for address decoding.
    - Used to generate the MCS16# signal.
- **DATA BUS (SD8-SD15): System Data (D15:8)**
  - These are the extra eight data lines needed for 16-bit transfers.

ISA 16-bit Connector Signals (Cont.)

ISA Conn. 36-Pin Portion: Logical Functions (cont.)

- **CONTROL BUS: MEMR#, MEMW#** (MRDC#, MWTC#)
  - Memory Read/Write Command
  - Active for Memory Accesses from 0-16MB.
  - Unlike SMEMR# and SMEMW# on the 62-pin adapter which were active for addresses below 1MB, these signals are active for all memory addresses.
  - 8-bit agents only receive SMEMR# and SMEMW# due to connector limitations.

ISA 16-bit Connector Signals (Cont.)

ISA Conn. 36-Pin Portion: Logical Functions (cont.)

- **INTERRUPTS**
  - Five new interrupt requests are added.
  - The slave 8259 has eight inputs, but three are used on the system board.
    - IRQ 8 -- Real-time clock chip (Alarm Output)
    - IRQ 9 -- Redirect to type 0AH (old IRQ 2)
    - IRQ 13 -- Coprocessor error
    - **The remaining five appear on the 36-pin connector**.

ISA 16-bit Connector Signals (Cont.)

ISA Conn. 36-Pin Portion: Logical Functions (cont.)

- **DMA (Direct Memory Access)**
  - The added DMA controller (DMA #2) has only three channels available, since the fourth channel is used in cascade mode to handle requests from DMA1.
    - **DRQ0, DACK0#-**-Channel 0 from DMA #1, 8 bit
      - **The DRQ4, DACK#4 lines used for cascade to the original DMA controller (DMA #1).**
  - New channels, 16 bit
    - DRQ5-7 -- Direct Memory Access Request
    - DACK5#-DACK7# -- Direct Memory Access Acknowledge.

ISA 16-bit Connector Signals (Cont.)

ISA Conn. 36-Pin Portion: Logical Functions (cont.)

- **ODDS AND ENDS**
  - **POWER**
    - +5V DC.
    - **0V DC--GND.**
  - **SBHE# - (System Byte High Enable)**
    - Asserted to indicate a transfer of data on the **D15:8** Data lines (**High Byte** of D15:0 Word).
    - Used with A0 to decode the type of bus cycle.
      - SBHE# = **0**, A0 = 0 -> **16 BIT** TRANSFER
      - SBHE# = **0,** A0 = 1 -> Upper Byte Transfer (**D15:8**) - Odd Addr
      - SBHE# = 1, A0 = 0 -> Lower Byte Transfer (D7:0)

ISA 16-bit Connector Signals (Cont.)

ISA Conn. 36-Pin Portion: Logical Functions (cont.)

- **ODDS AND ENDS - TRANSFER SIZE**
  - **MCS16# -- Memory Cycle Select 16-bit (M16#)**
  - **IOCS16# -- I/O Cycle Select 16-bit (IO16#)**
    - Indicates the adapter card can support 1 wait state 16 bit transfers on the present cycle.
    - **These two signals permit a 16-bit memory or I/O device to request that the system board run a 16-bit bus cycle on the I/O channel.**
    - NOTE: The ISA BUS defaults to running 8-bit cycles, even if the CPU is transferring 16 bits. The default assumes the transfer is to an XT type adapter.

ISA 16-bit Connector Signals (Cont.)

ISA Conn. 36-Pin Portion: Logical Functions (cont.)

- **ODDS AND ENDS**
  - **MASTER# (MASTER16#)**
  - An adapter card can become a limited bus master in the PC/AT.
  - An adapter card wishing to be a bus master takes these steps:
    - 1. Make a DMA request on one of the available DMA channels.
    - 2. After receiving the corresponding DACK#, the adapter now activates the MASTER# signal (active low).

Cont. next page

ISA 16-bit Connector Signals (Cont.)

ISA Conn. 36-Pin Portion: Logical Functions (cont.)

- **ODDS AND ENDS**
  - **MASTER# (cont.)**
    - 3. The adapter can now drive the address, data, and control signals.
      - » MASTER# causes the System Board to turn around bus buffers so the ISA card can drive addresses & bus cycle definitions.
    - 4. To permit memory refresh, the adapter must either drive the REFRESH# signal every 15.6 us or release the MASTER# and the DRQ signals.
      - » The system board actually does the refresh cycle in either case.

ISA BUS CYCLES

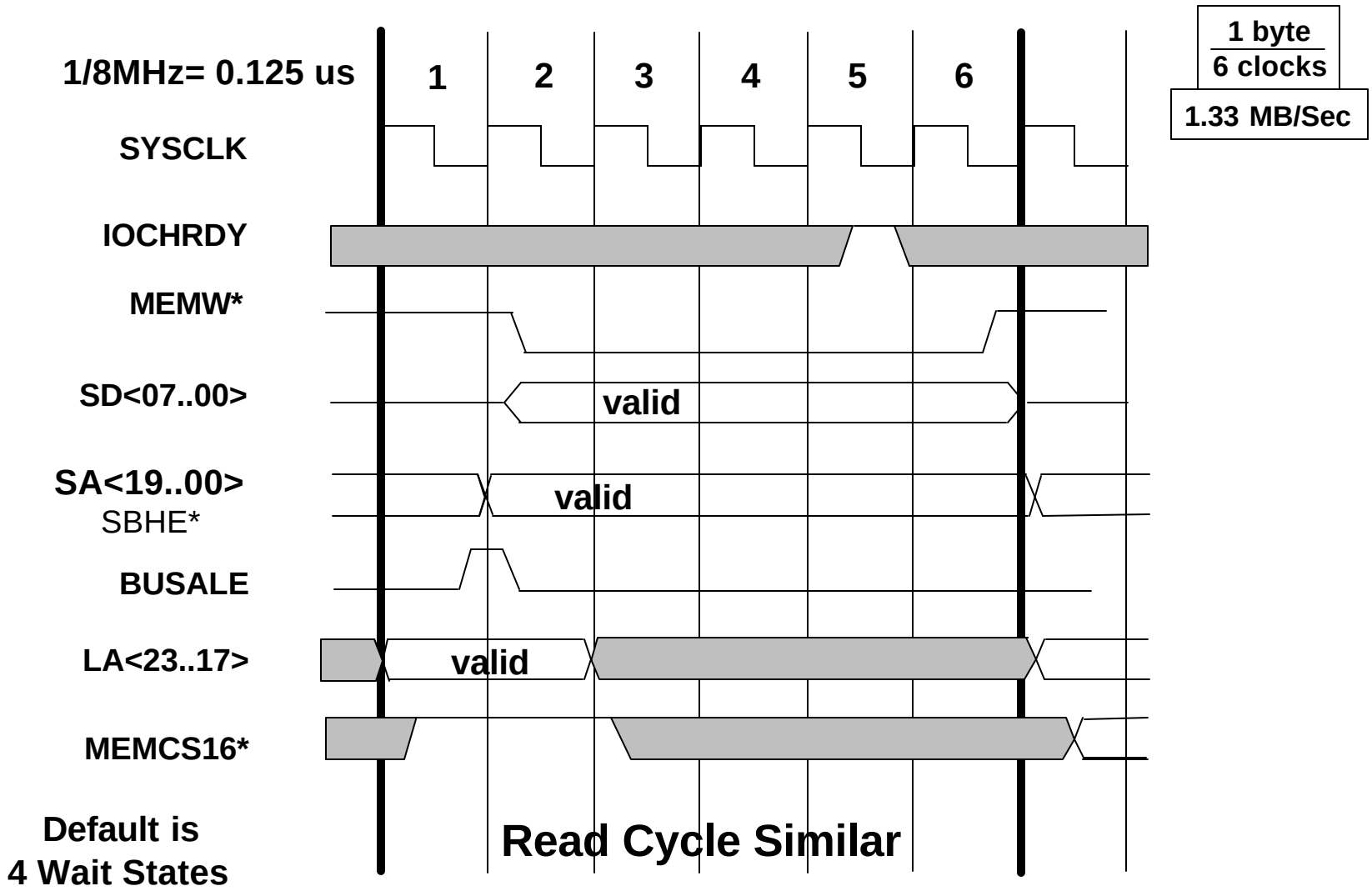
ISA BUS CYCLES

- This section discusses the following topics on ISA bus cycles.
  - 8-bit memory cycles
  - 8-bit I/O cycles
  - Conversion cycles
  - 16-bit memory cycles
  - 16-bit I/O cycles
- The system board contains logic integrated into chip sets that execute bus cycles on the ISA bus.
- These bus cycles look very much like the typical system bus cycles we have seen already.

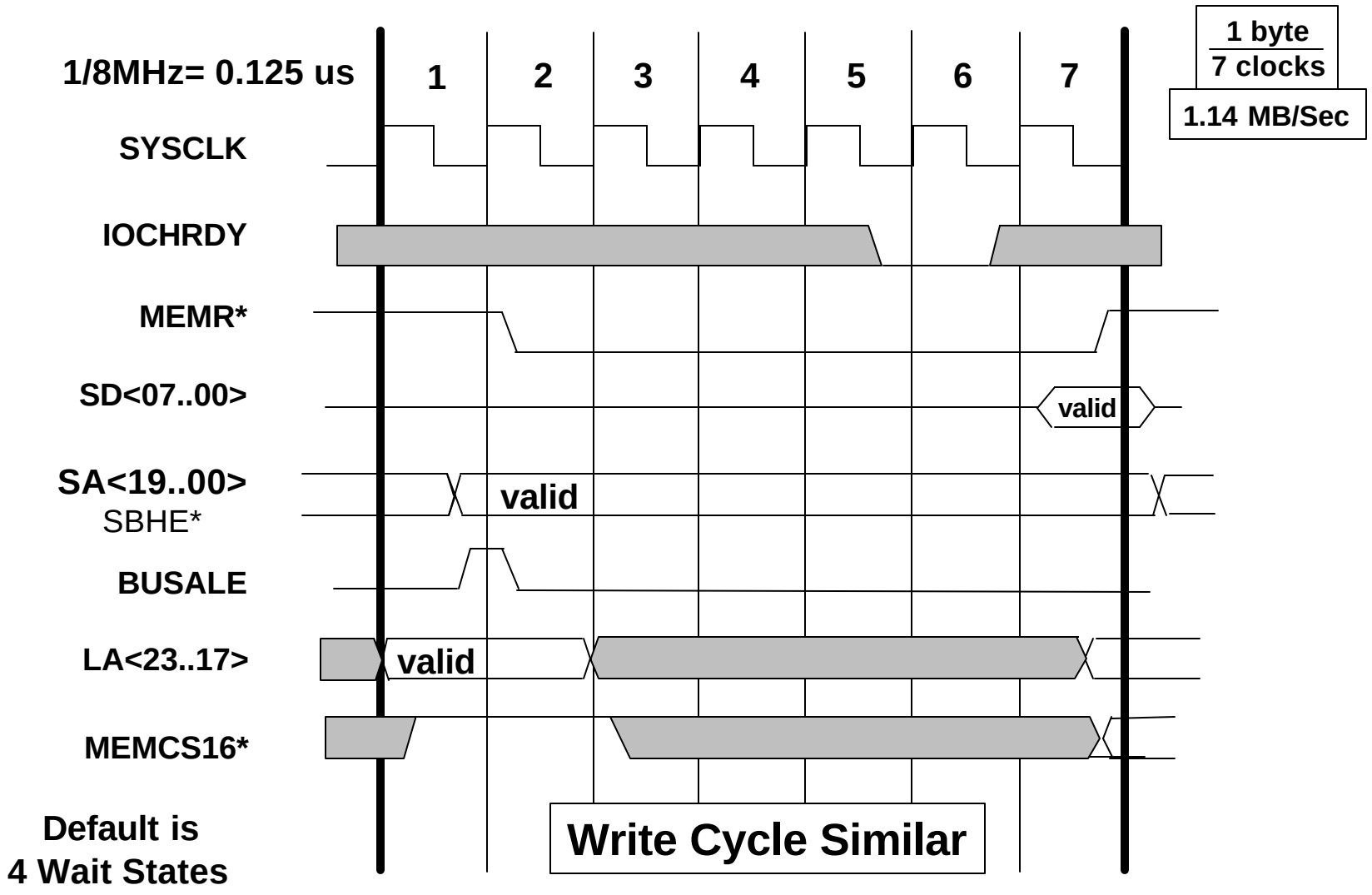
HISTORY OF ISA BUS CYCLE TIMING

- **The ISA bus cycle timing was originally dictated by the 8088 CPU running at 4.77 MHZ.**
- The PC/AT I/O channel bus cycle timing included wait-states to lengthen the inherent 286 bus cycles.
  - The original PC/ATs had a CPU clock of 6 MHZ, later increased to 8 MHZ.
- The PC/AT's 8-bit cycles matched closely those of the PC/XT for compatibility. The 8-bit cycles included 4 wait-states.
- The PC/AT's 16-bit cycles included a default wait-state to allow adapters to use slower memory.
- Timing Diagram reference Intel Doc# 458057-001.

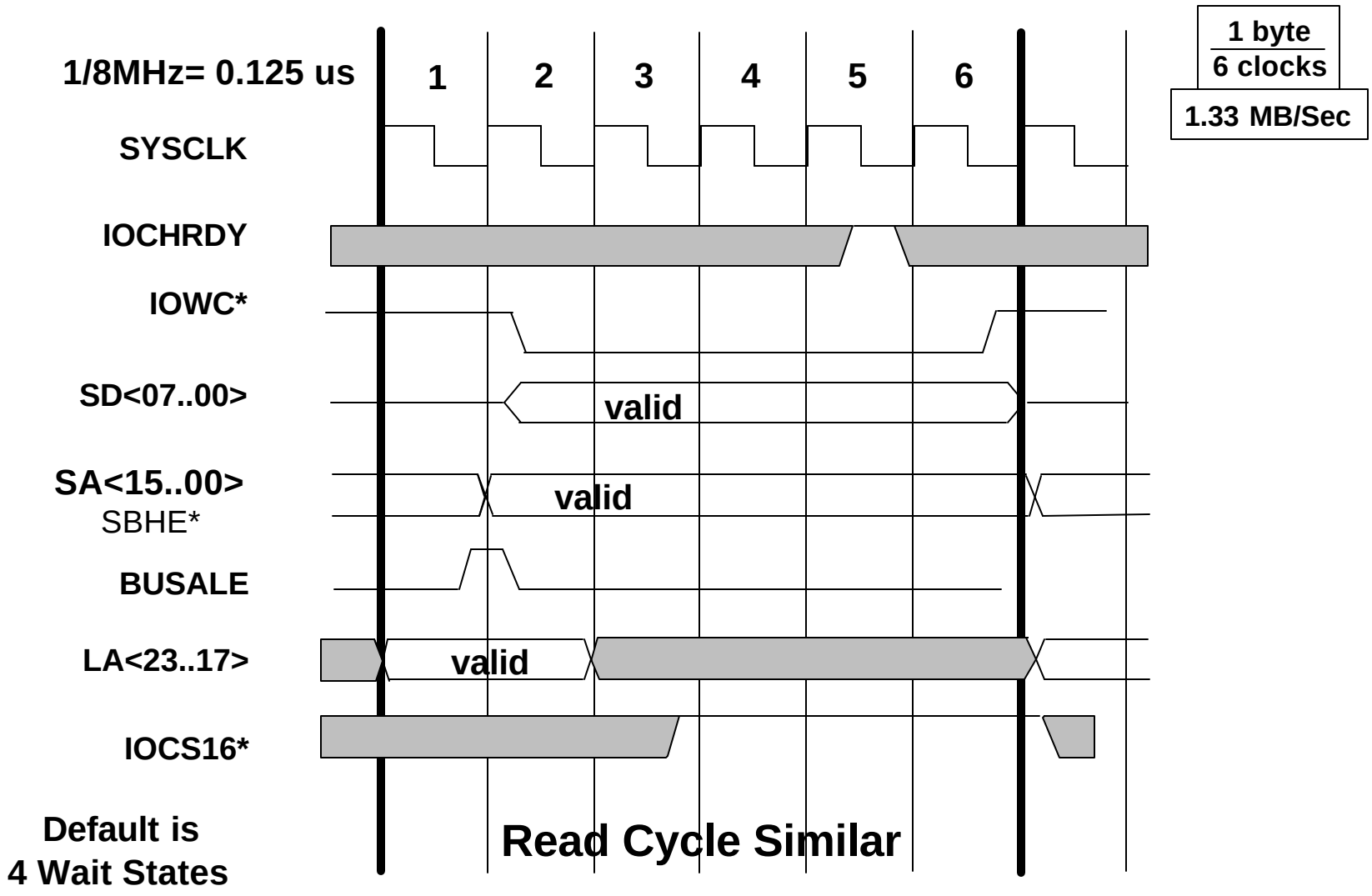
Standard 8-bit Memory Cycle (Write)



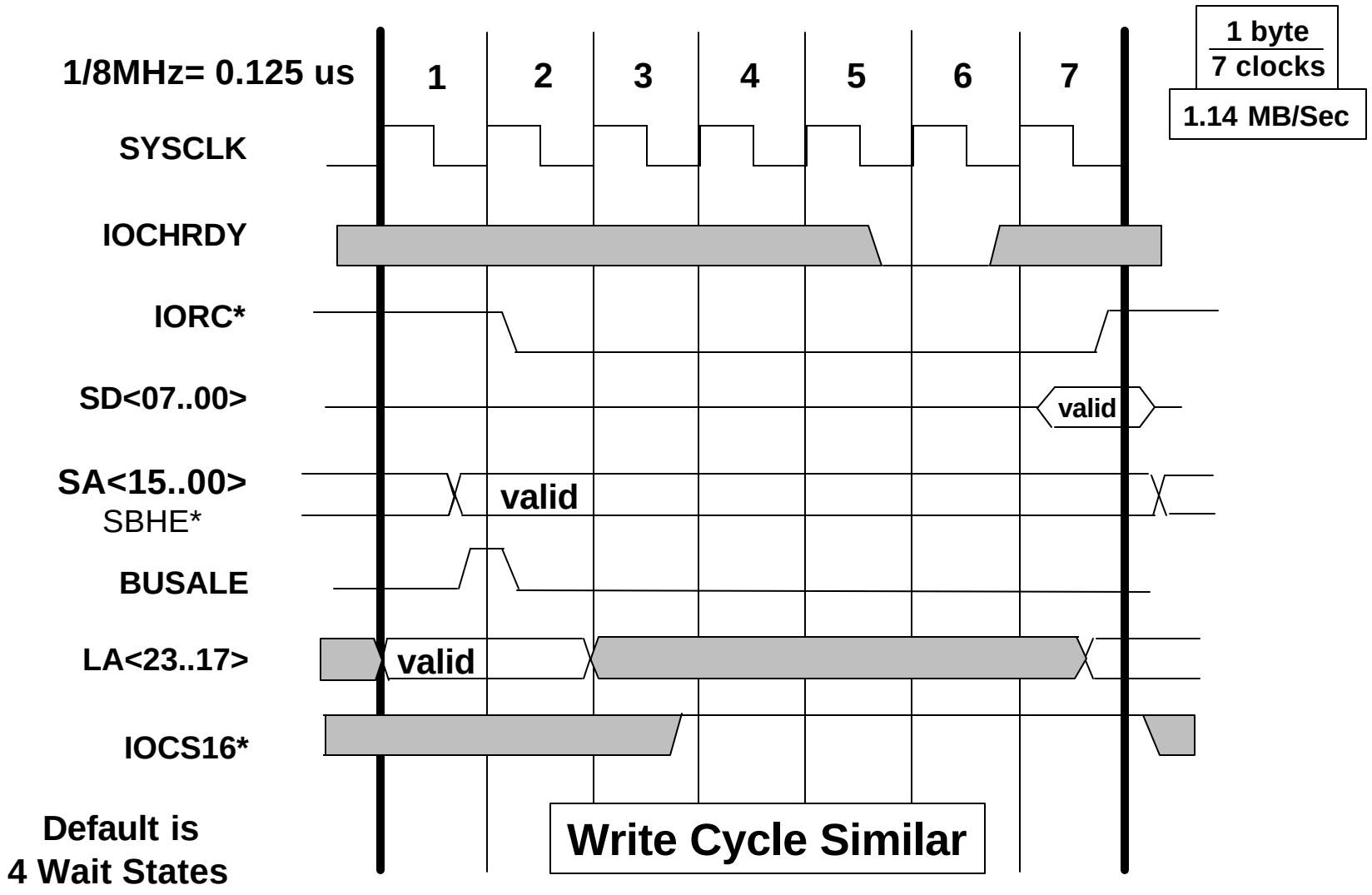
(Add 1 Wait State) 8-bit Memory Cycle (Read)



Standard 8-bit I/0 Cycle (Write)



(Add 1 Wait State) 8-bit I/O Cycle (Read)



CONVERSION LOGIC

- To make the PC/AT backward compatible with PC/XT memory and I/O boards, the PC/AT system board contains logic to **convert 16-bit bus cycles to two 8-bit bus cycles.**
- **NOTE: The Conversion Cycle is the Default**.
  - The conversion cycle can be overridden by the use of #MCS16 or IOCS16#.

CONVERSION LOGIC

- **Example:**
  - An instruction causes the CPU to run a 16 bit Memory Write bus cycle.
  - Suppose however, that target of the write is on an 8-bit memory card, connected only to DO-D7.
- The conversion logic will capture the 16 bits coming from the CPU and run two 8-bit bus cycles on the ISA BUS.
  - During the first bus cycle, the low byte is put directly on D0-D7.
  - During the second bus cycle, the high byte is swapped from the upper 8 data lines on the system board to D0-D7 on the ISA bus.

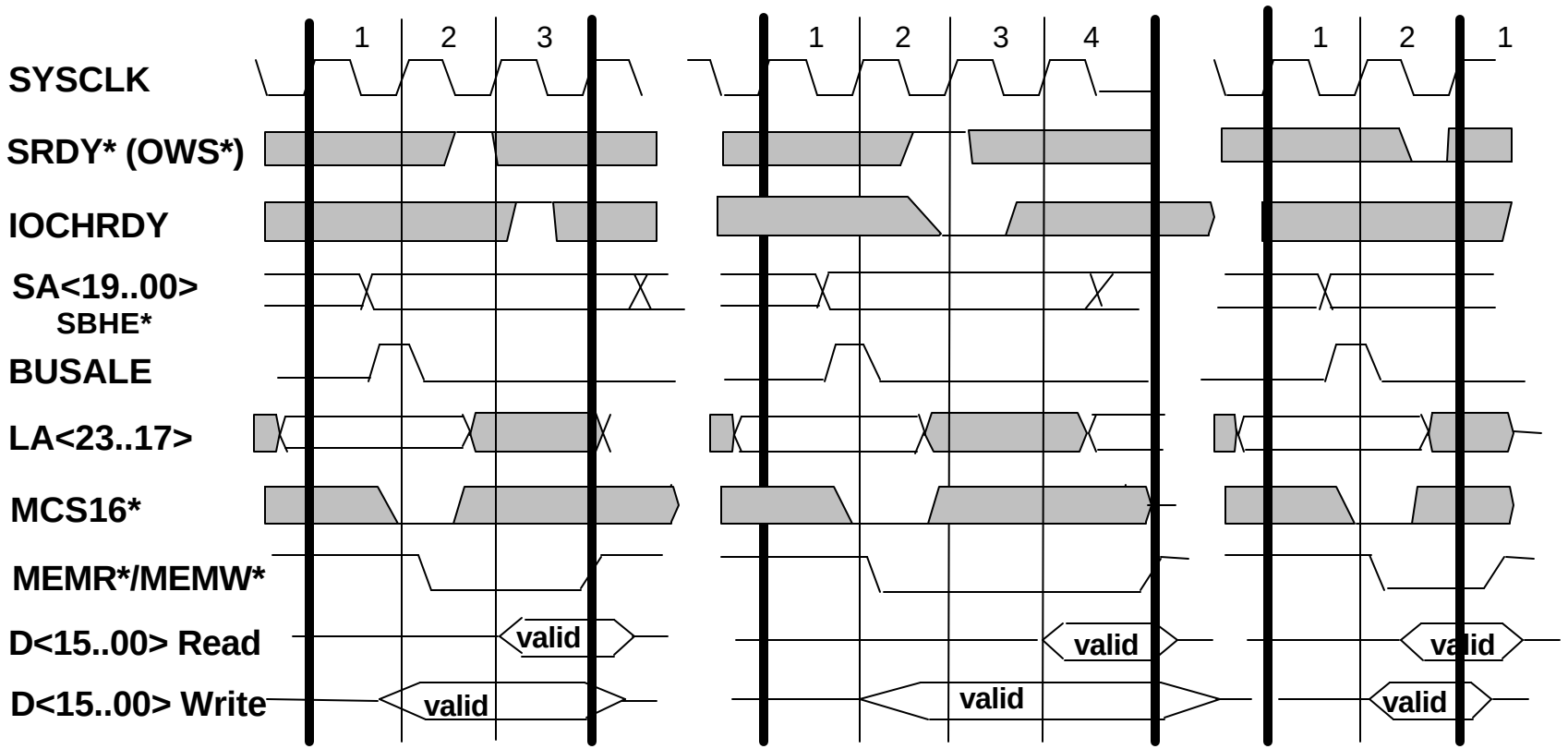
16-bit Memory Cycle (STD, Add 1 WS, OWS)

Default is 1 Wait State

2 bytes / 3 clocks
5.33 MB/Sec

2 bytes / 0.25 us
8.0 MB/Sec

1/8MHz= 0.125 us



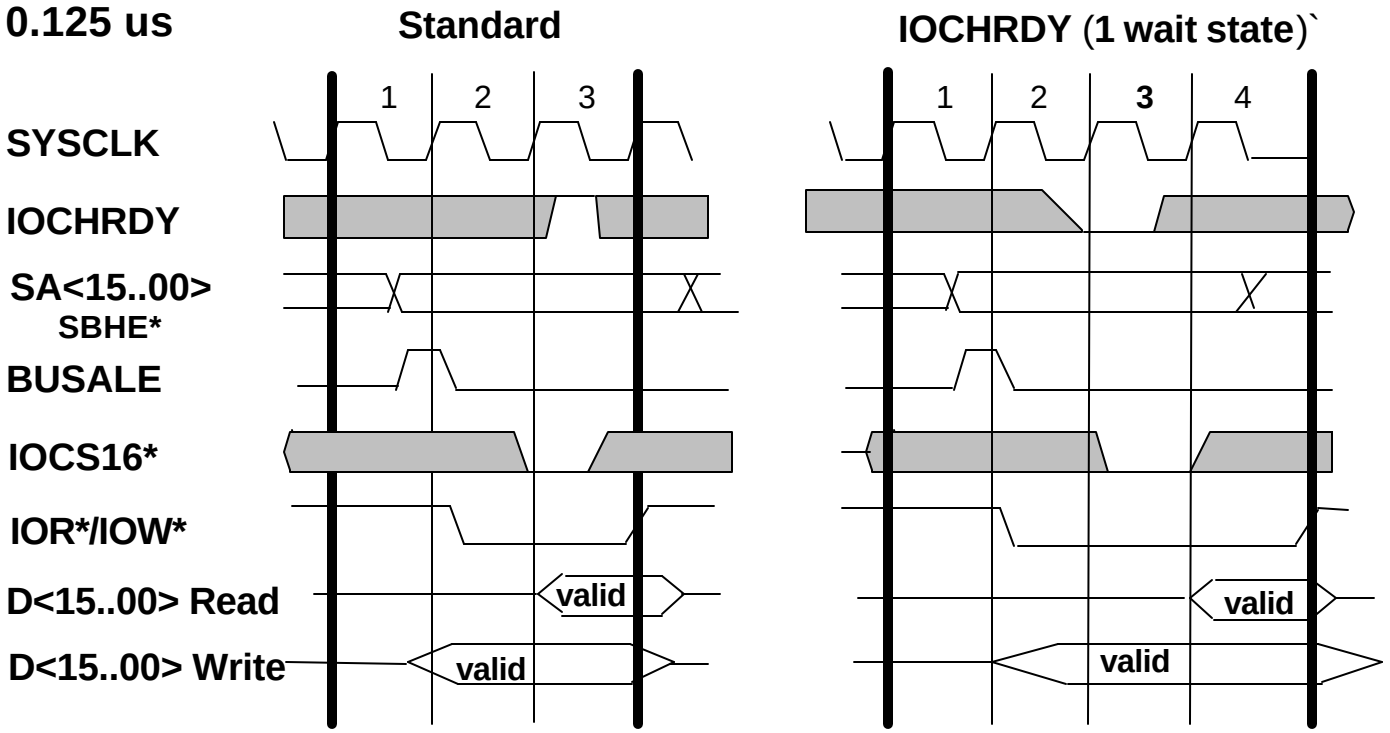
16-bit I/O Cycle (STD, Add 1 WS)

Default is
1 Wait State

2 bytes / 3 clocks
5.33 MB/Sec

2 bytes / 0. 5 us
4.0 MB/Sec

1/8MHz= 0.125 us



SUMMARY

WE HAVE DISCUSSED THE FOLLOWING:

- **The functions of the Industry Standard ISA Expansion Bus.**
- **Typical System Bus Cycles.**
- **The Functions of the Signals on the I/O Channel.**
- **The ISA BUS Signal Descriptions.**
- **8-bit Memory & I/O ISA BUS Cycles.**
- **Conversion BUS Cycles.**
- **16-bit Memory & I/O ISA BUS Cycles.**