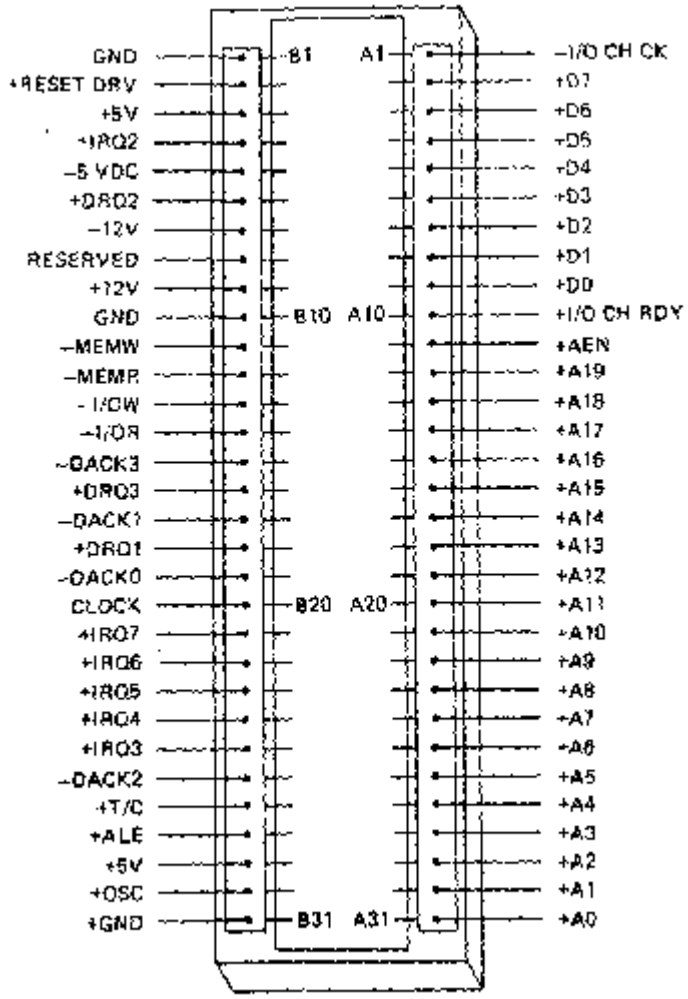
ISA Bus - A Brief Description and IO Device Design

The purpose of this web page is to introduce you to the PC ISA bus and to show you how to do simple IO designs using this bus. First, consider a picture of the bus shown below.



ISA Pin Descriptions

DATA - Lines D0-D7 form the biirectional data bus. The data bus is driven by a bidirectional buffer that is only enabled at times corresponding to data availability (iowc/, iorc/, memw/, memr).

ADDRESS - Output lines A0-A19 form the address bus. These lines are fully demultiplexed and stable during a full bus cycle.

ALE - Address Latch Enable - This output signal comes directly from the bus controller IC and provides timing information for decoding the address lines. It is not needed for bus decoding since the address lines are already demultiplexed on the ISA bus.

AEN - Address Enable - This output signal allows the IO device to distinguish between processor bus cycles and DMA bus cycles. A high on AEN indicates that a DMA cycle is occuring and that the address, data and control lines are under the control of the DMA controller. Peripheral IO devices that do not have DMA capability should insure that they only decode address that are generated by the processor (AEN='0') and not a DMA controller.

IO CHANNEL RDY - This normally high input line can be pulled low by a slow device to inserve wait states.

IO CHANNEL CHECK - This normally high input line is pulled low to indicate a memory or IO device pari6ty error. In turn, the parity error will cause a non-maskable interrupt (NMI) of Type 2 to occur.

RESET DRV - This output signal is active high during power-on and can be used to reset or initialize IO devices.

DRQ1-DRQ3 - These input lines are connected to the corresponding DMA request pins on the DMA controller. Raising a selected line generates a DMA request. DMA channel 0 is reserved for memory refreshing.

DACK0-DACK3 - These four active low output lines provide DMA acknowledge signals for the four DMA channesl. DACK0 can not be used by other devices but is useful since it indicates that a DRAM memory refresh cycle is occuring.

IRQ2-IRQ7 - Interrupt request lines are connected directly to the PC interrupt controller. A line should be held high until the request is serviced by the appropriate interrupt service routine. IRQ0 and IRQ1 are reserved for use on the system board by the time of day and keyboard interupts and are not generally available. Other lines may be used by other devices as well.

OSC - The output of the system oscillator, typically around 8-20MHz (traditionally 14.318MHz).

CLK - Traditionally the processor clock signal with a 33% duty cycle (4.77MHz). More recent PC systems will have frequencies in the range of 4-10MHz. The frequency of this clock output should always be measured to insure that it is used properly.

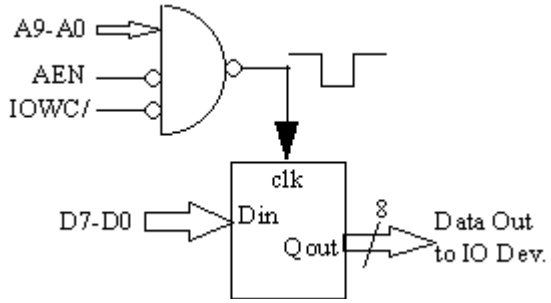
Power Supply Lines - All voltages available on the system board are available on the ISA bus. These include +5Vdc and ground, +12 and -12Vdc, and -5Vdc. The current draw from each of these lines should be carefully controlled.

Interface Design

- Any IO device interfaced to the PC bus must decode an address, decide whether the address is originating from the host processor or a DMA device, determine the direction of data transfer and, if appropriate, either accept data or provide data at the proper time.
- The minimum set of signals that must be used in an interface design are: AEN, A0-A9, IOWC/ and IORC/.
- ADDRESS Decoding - AEN and A0-A9 are used to decode a 10 bit ISA address generated by the processor. AEN must be low. Only A0-A9 are used for IO address (*not* memory address) decoding by convention with the original PC. The upper address lines are ignored.

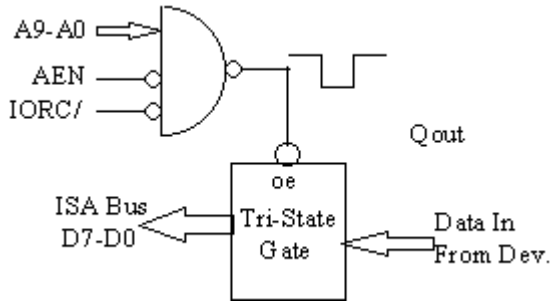
- IOWC/ and IORC/ are used in conjunction with address decoding to generate a device select pulse (DSP) that can be used to strobe data into a latch (IOWC/) or enable data onto the data bus (IORC/) to be read by the host processor.

Simple Output Port Design



Note in this design that you need an address decoder that produces a negative true output pulse (the NAND gate) in response to a selected address (probably in the range of 300-330h) and only when AEN is low and IOWC/ is low. The trailing edge of the DSP signal goes into the clock strobe of the 8 bit latch and is used to latch the data from the ISA bus at the correct time.

Simple Input Port Design



The design for an input port is similar to the design for an output port with the exception that you need an 8-bit tri-state gate to buffer the data from the IO device to the ISA bus. The gate is an essential component and is there to protect the ISA bus from being driven at the wrong time. The address and control signal decode logic provides the Read device select pulse signal (negative true) that determines when data from the IO device is passed to the ISA data bus to be read by the processor.

Created and maintained by F. Looft, Dept. of Electrical and Computer Engineering
Worcester Polytechnic Institute, Worcester MA 01609
email: fjlooft@ee.wpi.edu fax: 508.831.5491