Am486 Microprocessor PCI Customer Development Platform

Am486 Microprocessor Development System With PCI Expansion and On-Board Am79C972 100MB/s Ethernet Controller

Table of Contents

Rev 1.0: Original design

Rev 1.1: Minor modifications after Design Review

Rev 1.2: Added External 8042 Style Keyboard Controller (SH24)
Removed Support for M1487 Internal KBC (SH15)
Removed Keyboard Interface From Clock Page (SH17)
Changed design name to Am486PCI C.D.P.

Rev 1.3: Added Extra Bypass Capacitors (SH5 & SH14 & SH15 & SH17)
Swapped Around Some Signals Within Resistor Networks (SH6 & SH20)
Renamed MCLK1 net to M_CLK1 (SH24)
Added 0-ohm resistor to make pin 10 & 11 pullup work (SH17)
Added Pin to HS1 for NetLister (SH3)
Fixed Error in 3.3V Regulator Circuit (SH12)

Rev 1.4: Rearranged Clock Nets to Facilitate Routing (SH17)
Changed Some Components to Standard Values
(50ohm to 49.9ohm, 1% on SH 13 and 40pF to 39pF,
5% on SH19)

Rev 2.0: Changed SIP resistor packs to 10-pin (SH2, SH3, SH11, SH15, SH16, SH17, SH19, SH20 & SH21)
Changed 330ohm SIP Resistor Pack to 8-pin (SH19)

SH3: Added diagram to correct Power Connector Footprint

SH4 & 5: Broke CPU Logic Analyzer Headers into 2 pages
Added PAL to gnerate CPU A0 and A1 and also generate a Logic Analyzer Qualify signal
Buffered BE[0..3], RDY#, BRDY#, and ADS# through the new PAL

SH9: Added better explanation of EIP Flash memory operation

SH11: Added configuration information for PCI slots
Removed circuit to generate PCI PERR# to cause
M1487 to assert NMI to Am486 microprocessor

SH13: Added a 4K serial EEPROM for user parameters and mux. circuit to daisy chain it off the 1K device.
'972 E/net device loads its configuration from 1K SEEPROM.
CLKCNTL signal from M1487 used to select 1K or 4K SEEPROM.

SH14: Swapped R107 and R109; R109 is 49.9ohm, 1%
Fixed wiring error on crystal

SH15: Added 5 more 0.1uF bypass capacitors for new chips ('F14, 'ABT125, 22V10, 'F08, 'C66)

SH16: Fixed wiring error on crystal
Fixed wiring error in generation of low-active reset signal RSTDRV#
Removed unused inverter (used on SH24)
Changed net on NMI pin to 1487NMI for use in new circuit
Changed R58 to be a populated component

Rev 2.0 (continued): SH17: Added jumpers to allow mulitple BIOS images in a single Flash ROM device
Removed 1 diode from VBAT generation circuit
Added new NMI generation circuit and spare 'F14 gates
Added jumper for external RESET# pushbutton

SH18: Fixed wiring error on crystal
Removed MCLK1 net (16MHz) and rewired MCLK2 to drive all 33MHz clock nets
Removed CLKCNTL signal from DOZE# pin of U17

SH20: Removed unneeded 0-ohm resistors from Super I/O chip
Fixed wiring error on crystal
Added 'ABT125 buffer to drive serial port LEDs

SH22: MACH device outputs changed for new ISA Flash support

SH23: Changed ISA Flash to 1MByte (512Kx16)

SH24: Removed unneeded logic from RTC interface
Added inverter to generate proper CS# for RTC chip
Fixed wiring error on crystal
Grounded U22-pin 22
Removed 1 unused OR gate for use on SH17

SH25: Switched mouse connector to verticle type
Changed 'F06 symbol to show o/c

Rev 2.1: Updated revision level and prototype warning on all sheets

SH17: Modified ROM jumpers to allow mulitple BIOS images in a single Flash ROM device and support 256K or 512K BIOS for non-PC applications

SH22: Added XBUSCSJ signal to Mach device so it does not respond when Am486 fetches the reset vector at FFFF FFF0

SH14 &15 &20: Connected pins 1 and 2 on all LEDs for greater purchasing/manufacturing flexibility

Rev 2.1A: SH1: New Rev. of cover sheet text; no design changes made!

SH7: Changed Cache Tag SRAM Speed to 10ns

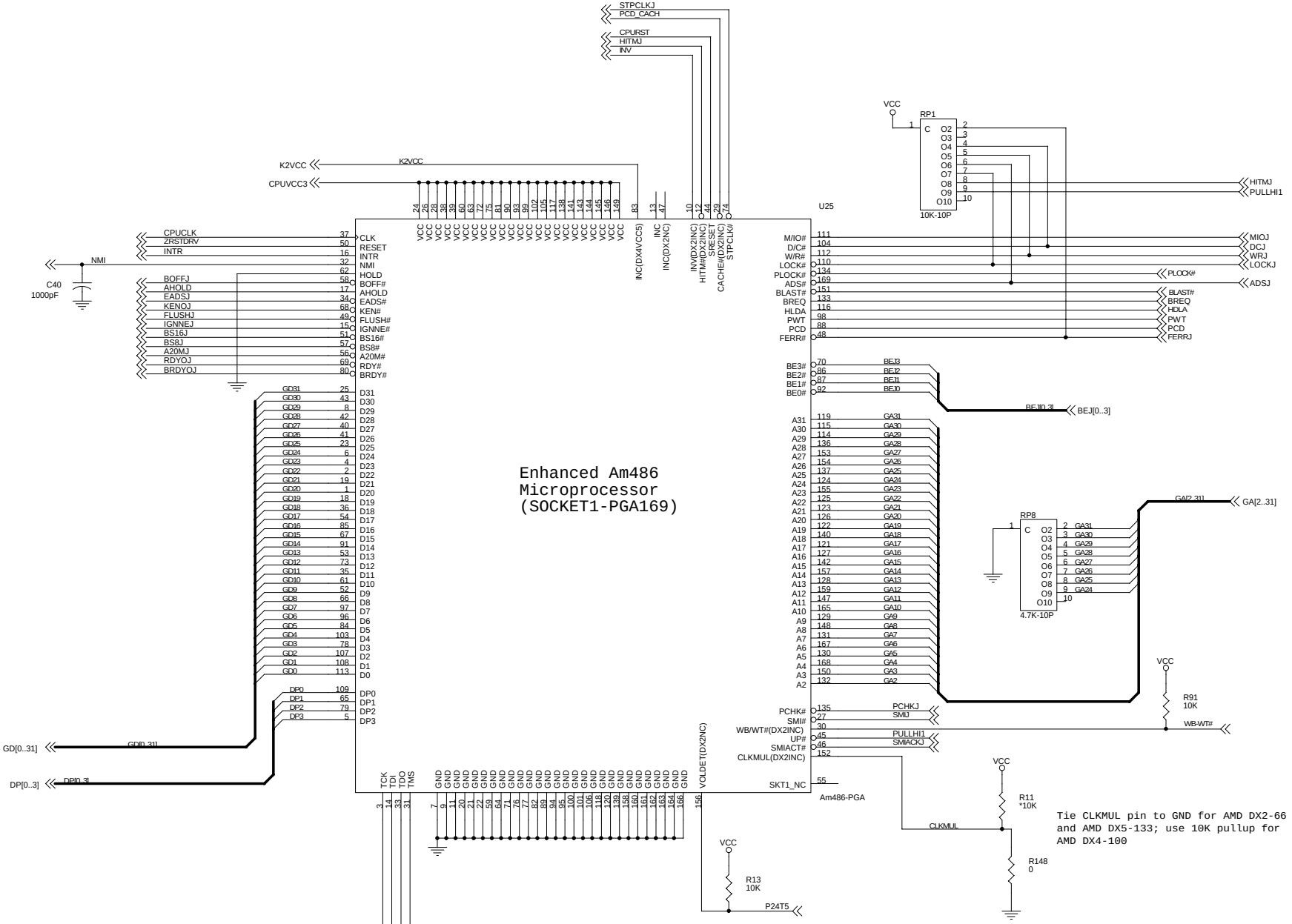
Note: Unless otherwise noted all logic operates off a 5V power supply

Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM	
Size	Document Number COVER.SCH	Rev 2.1A
Date: Friday, December 18, 1998	Sheet 1 of 26	

Am486 MICROPROCESSOR, PULLUPS, AND JTAG INTERFACE

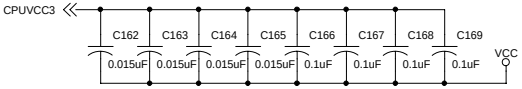


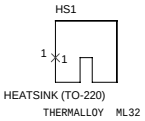
(C) Advanced Micro Devices, Inc. (800) 222-9323

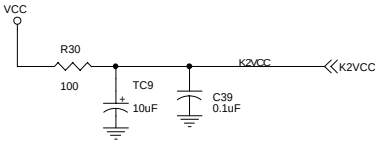
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved

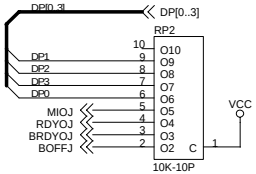
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM	
Size	Document Number CPU.SCH	Rev 2.1
Date: Friday, December 04, 1998	Sheet 2 of 26	

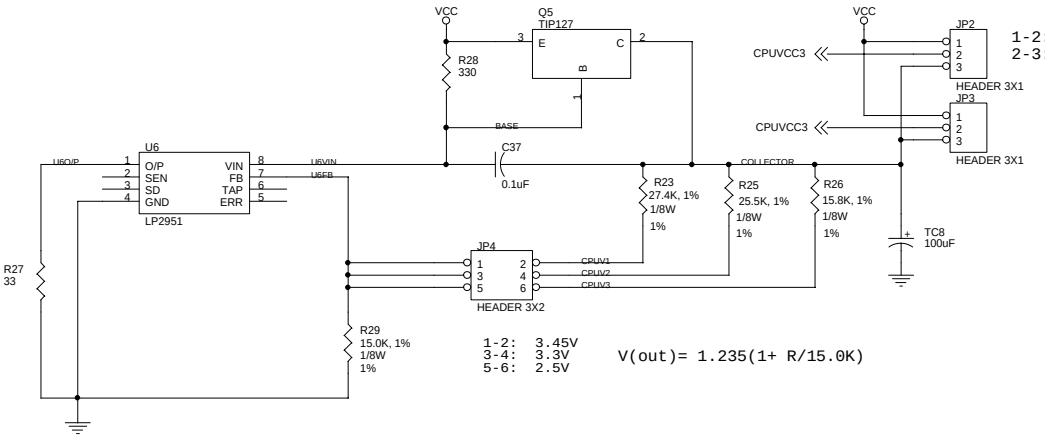
POWER CONNECTOR, CPU PULLUPS, CPU POWER SUPPLY, CPU BYPASS CAPACITORS

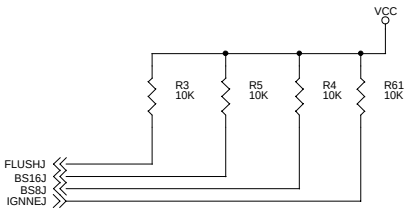


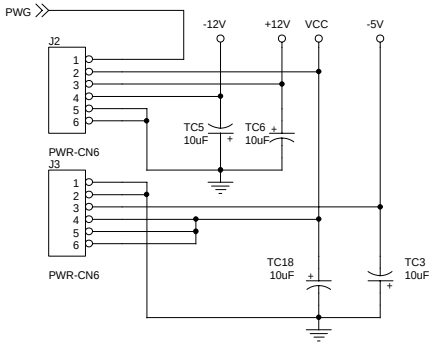


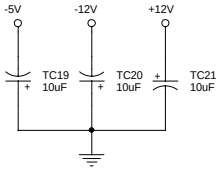


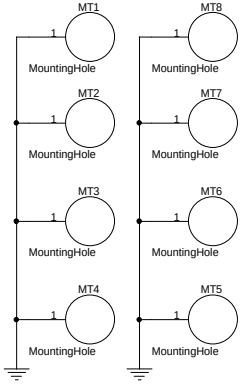


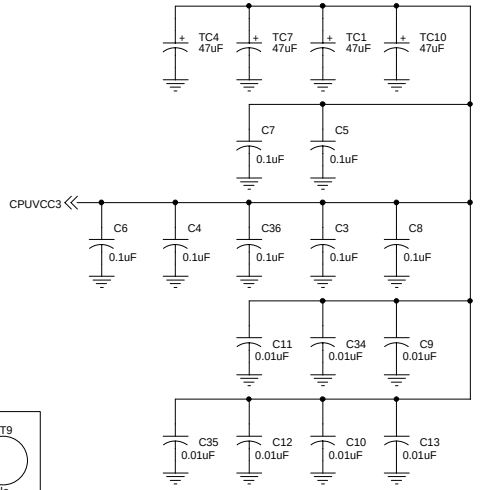


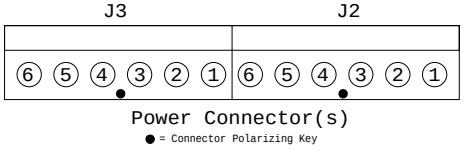










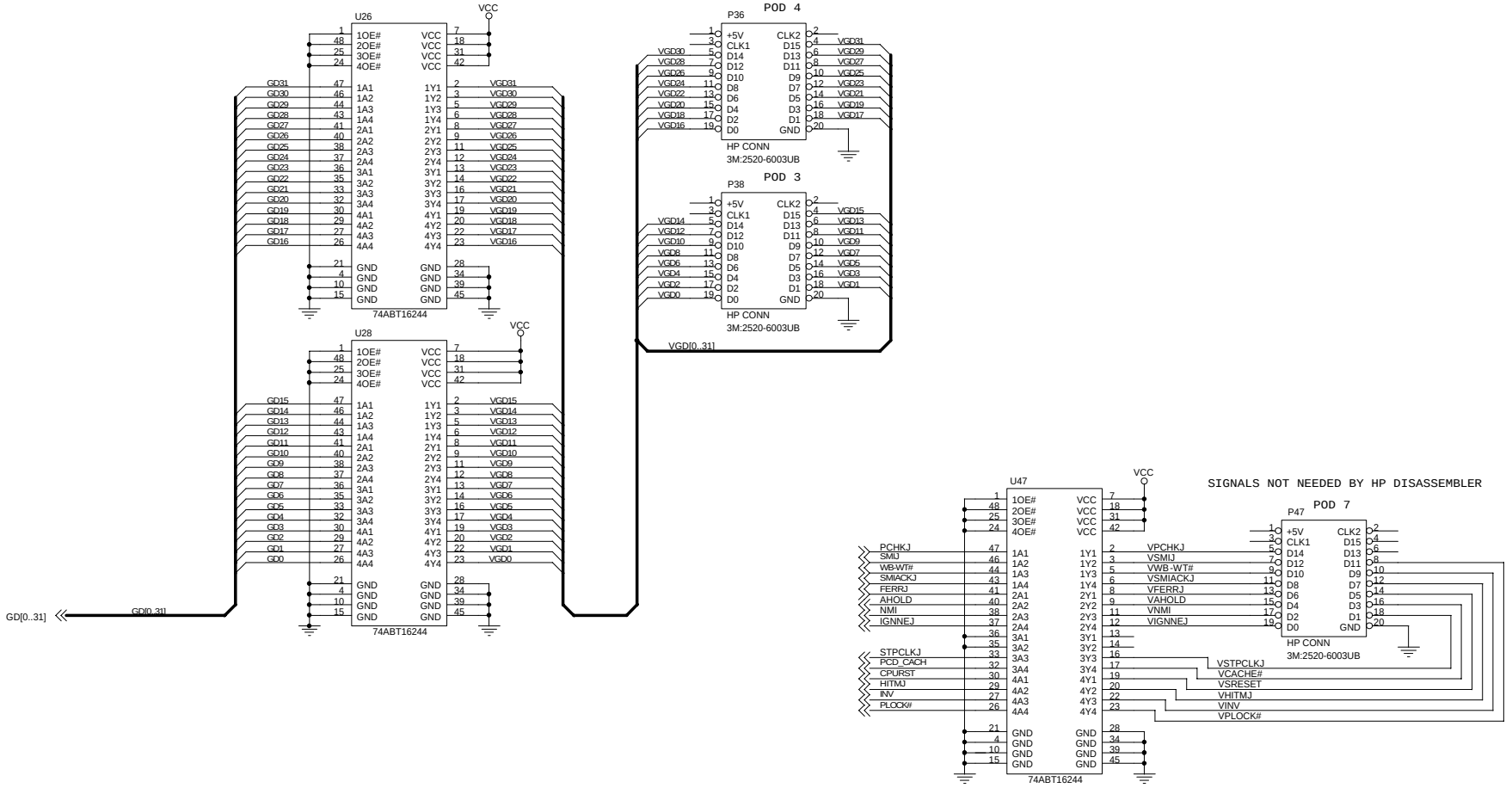


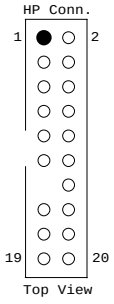
Power Connector(s)

● = Connector Polarizing Key

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: CPU_POWER.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 3 of 26

BUFFERS AND LOGIC ANALYZER HEADERS FOR CPU SIGNALS





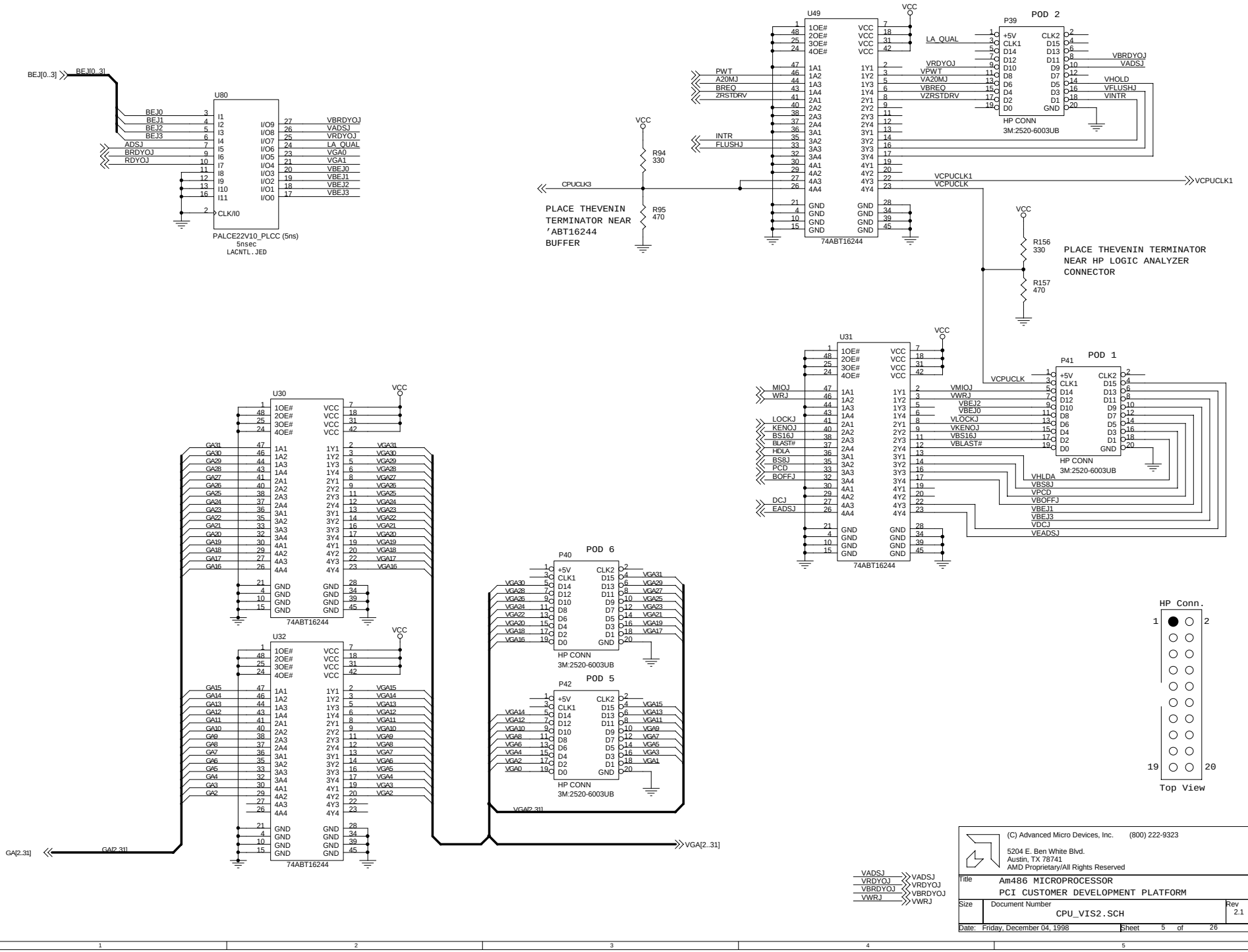
Using Logic Analyzer Headers:

Clock the analyzer off the clock signal on P41 (POD1)

Qualify the clock using the LA_QUAL signal on P39 (POD2)
This qualification signal is asserted (1) when ADS#, RDY# or BRDY# is asserted on the Am486 Microprocessor bus.
Thus cycles where valid address or data information is not transferred can be filtered out when needed
Signals are arranged on the LA Headers to work with the HP Disassembler for the 16500 analyzer

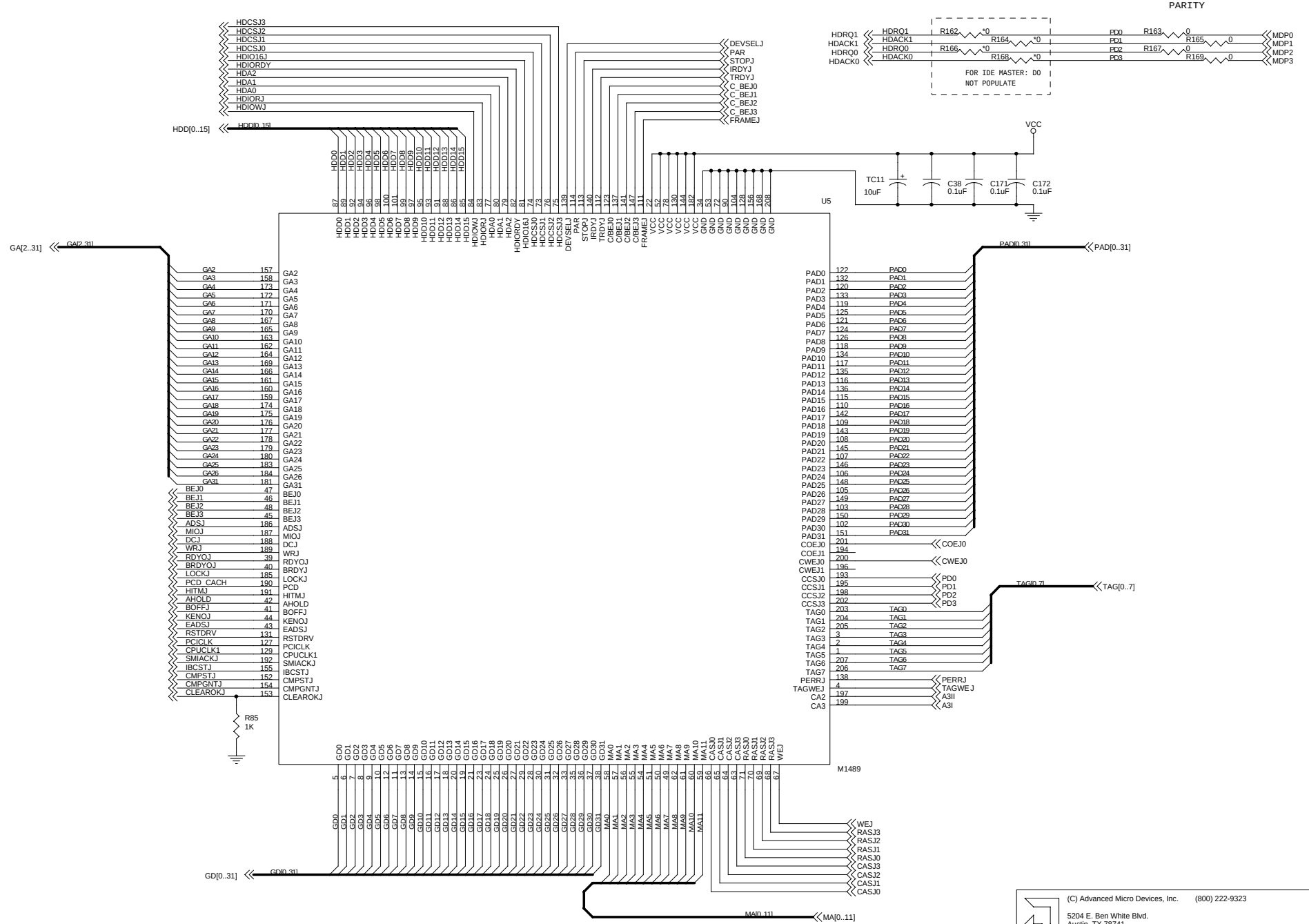
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: CPU_VIS1.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 4 of 26

BUFFERS AND LOGIC ANALYZER HEADERS FOR CPU SIGNALS, AND PAL TO AID LOGIC ANALYZER USE



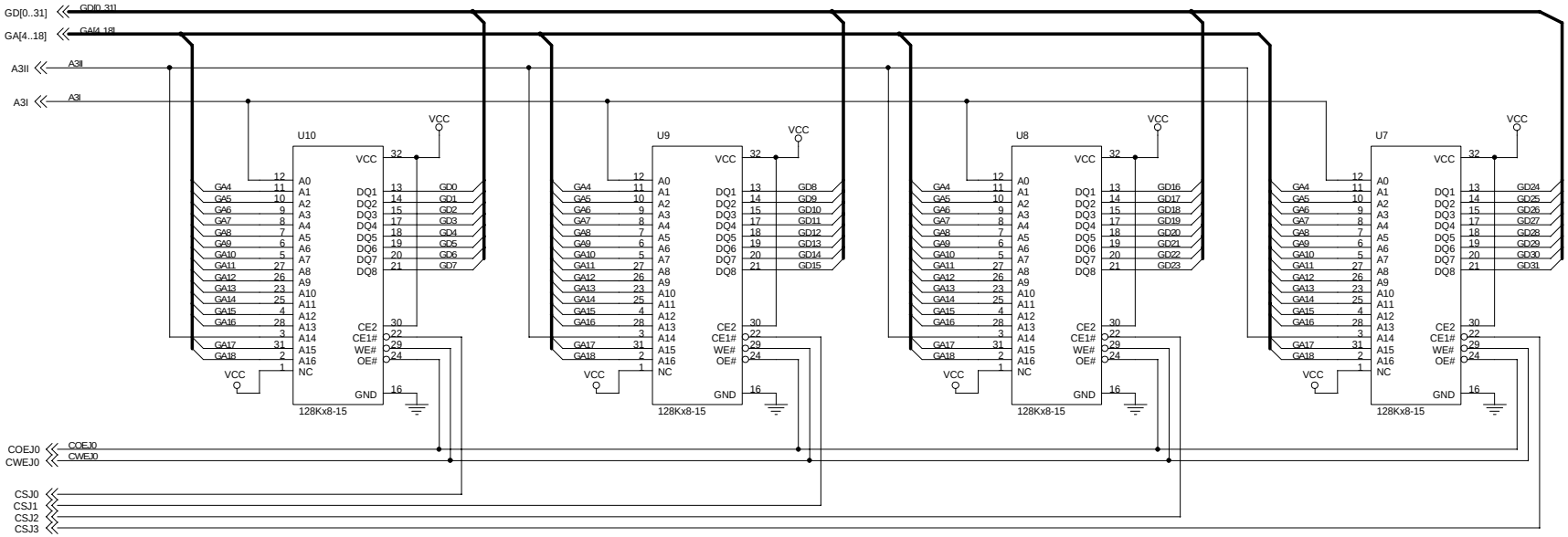
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM	
Size	Document Number CPU_VIS2.SCH	Rev 2.1
Date: Friday, December 04, 1998	Sheet 5 of 26	

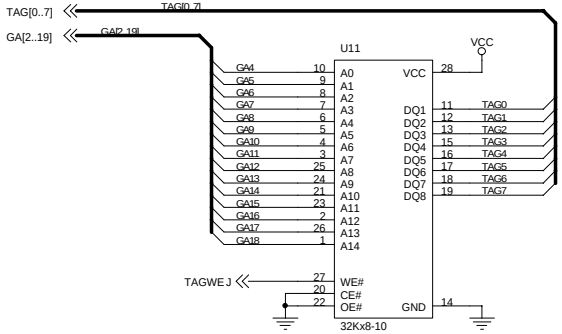
FINALi M1489 INTERFACE

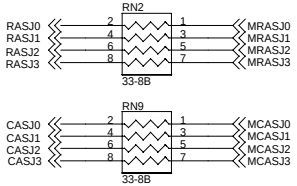


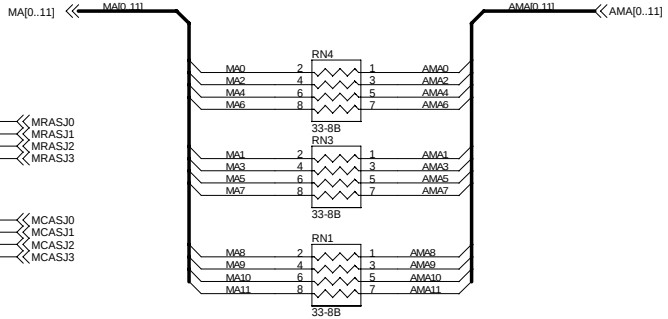
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: M1489.SCH — Rev: 2.1
Date: Friday, December 04, 1998	Sheet 6 of 26

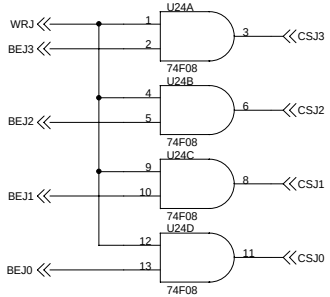
L2 CACHE TAG AND DATA SRAMS AND BYTE CONTROL; DRAM SERIES TERMINATION AND WE* FANOUT

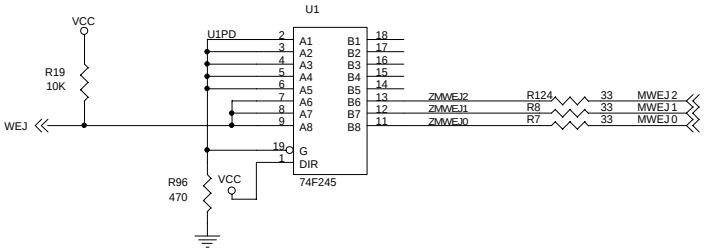






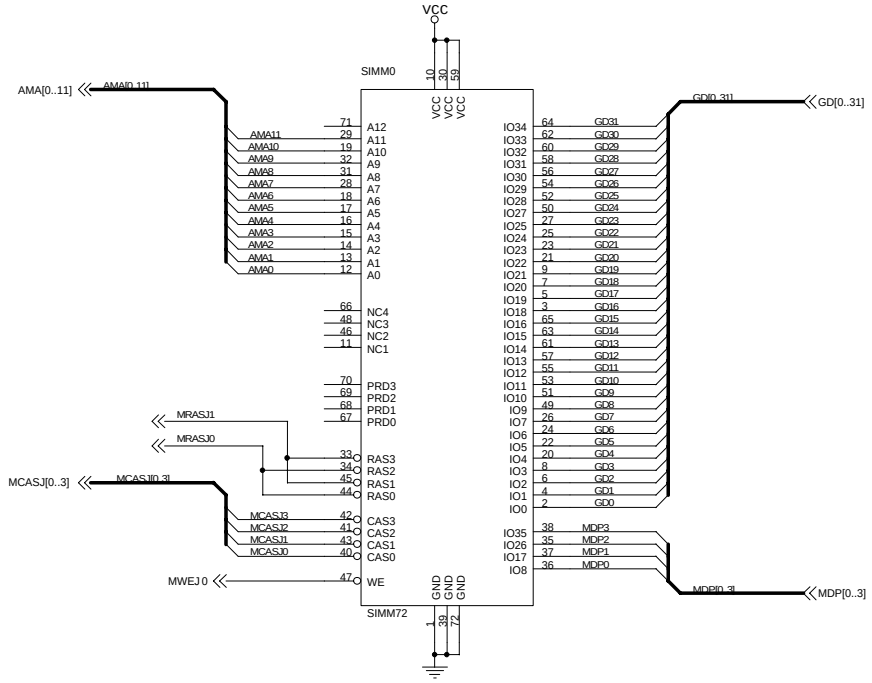


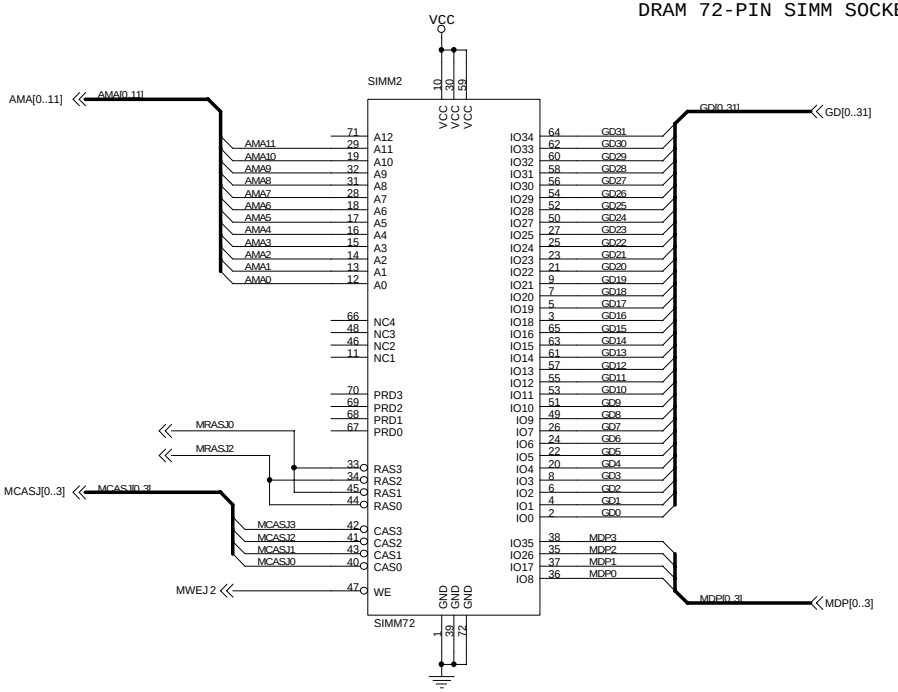


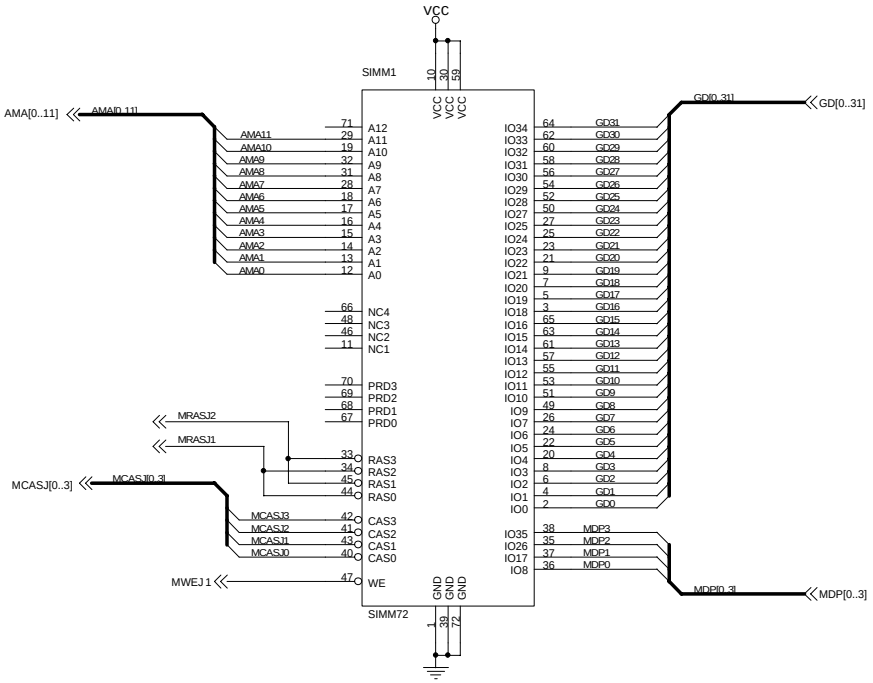


Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: L2_CACHE.SCH — Rev: 2.1A
Date: Friday, December 18, 1998	Sheet 7 of 26

DRAM 72-PIN SIMM SOCKETS







SIMM SOCKET POPULATION CHART

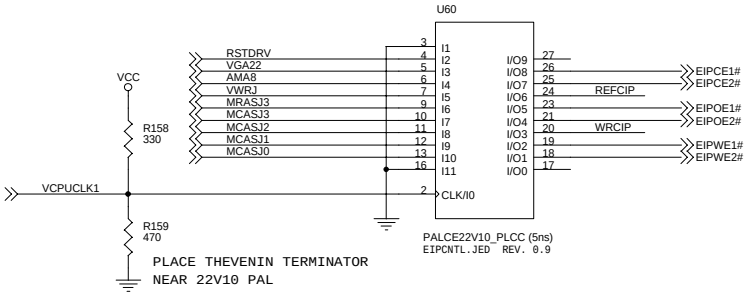
SIMM0	SIMM1	SIMM2
SINGLE BANK	SINGLE BANK	SINGLE BANK
DOUBLE BANK	SINGLE BANK	

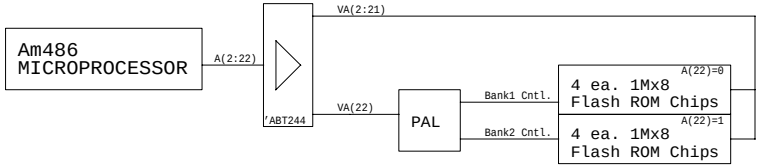
SIMMS CAN BE SINGLE BANK OR DOUBLE BANK, USING
1Mbit, 4Mbit, or 16Mbit DRAM CHIPS. POPULATE
SIMM SOCKETS AS SHOWN IN THIS CHART.

Title: Am486 MICROPROCESSOR
PCI CUSTOMER DEVELOPMENT PLATFORM

Size | Document Number: SIMM_SKTS.SCH | Rev: 2.1

Date: Friday, December 04, 1998 | Sheet 8 of 26





CPU Address Bit A(22) Used As Flash Bank Select

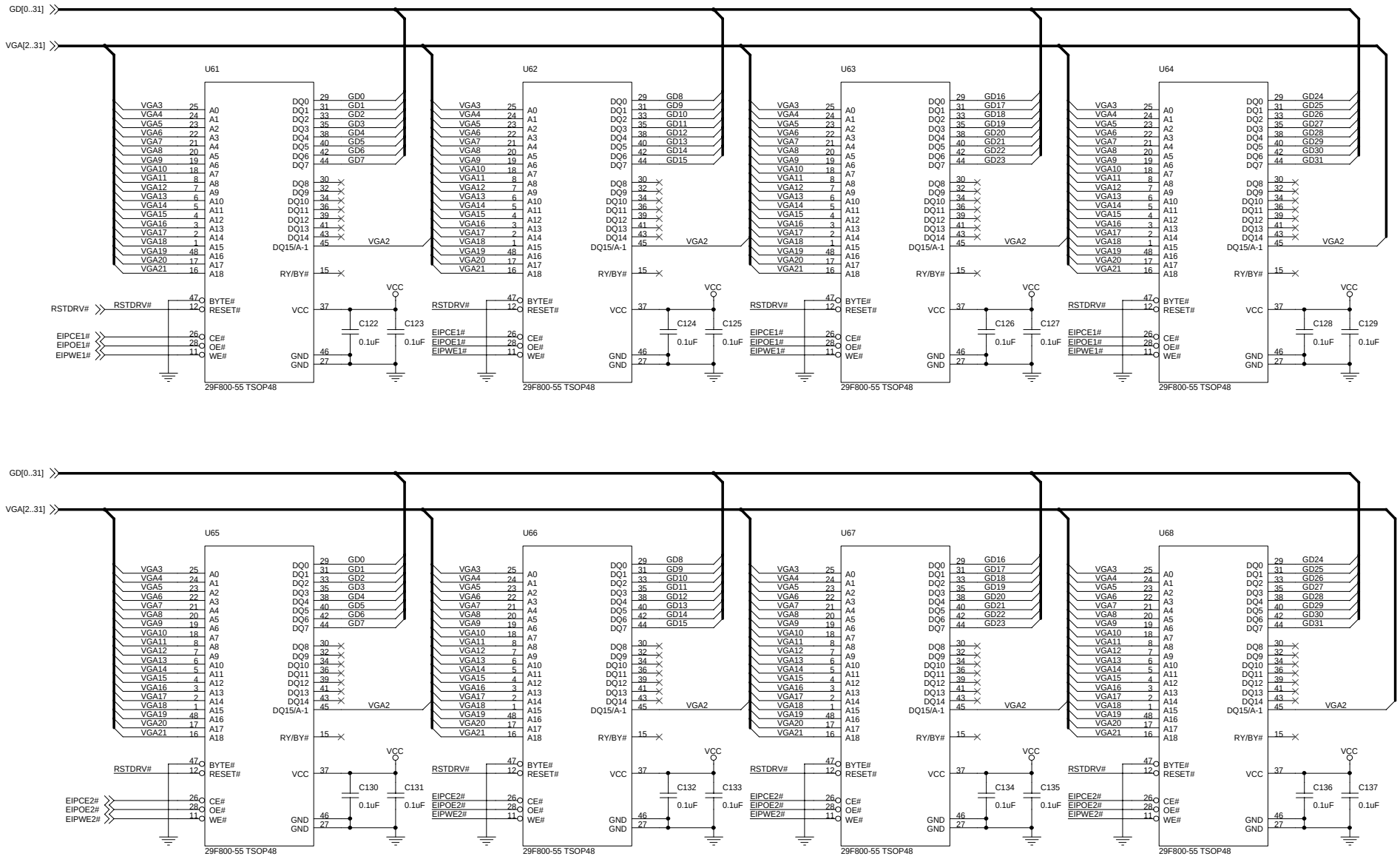
Makes 2 banks of 1Mx32 Flash ROM appear as 1 bank of 2Mx32 DRAM (70ns, FPM) to M1489 Memory Controller. Program M1489 for 2Mx8 (11/10) DRAM chips. MA8 (CPU A22) used as Flash ROM Bank Select when RAS3# asserted by M1489 Memory Controller.

Limitations and Operation of the EIP Interface:

- Access as 32-bits wide always
- Supports burst Read Cycles or single-beat Read Cycles
- Supports single-beat Write Cycles only; no back-to-back Write Cycles
- Compatible with CAS-before-RAS Refresh Cycles only
- Set M1489 Memory Controller to "Fast" for proper operation, even if installed DRAM is 60ns and can run at the "Fastest" setting
- Flash chip A0 pin tied to Am486 Microprocessor A2 pin, so multiply desired Flash chip address by 4h to find Am486 Microprocessor address needed to access the desired memory cell (ex: Flash Chip AAAh accessed by Am486 Microprocessor at 2AA8h)
  EIP Flash Array start address moves, depending on how much DRAM is installed (ex: 48MByte DRAM puts EIP start address at 48MB or 3000000h for first bank of Flash ROMs and 3400000h start address for second bank of Flash ROMs
  Uses 29F800T, 55ns devices in "Byte" mode
- Accessable from Am486 Microprocessor only; not accessable from PCI Bus Masters
- Uses fourth DRAM bank of M1489 Memory Controller

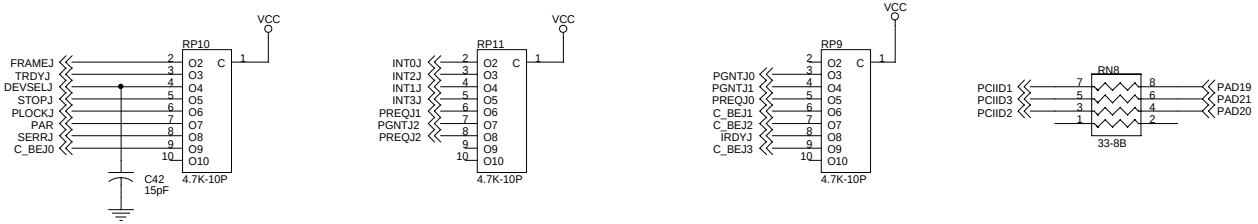
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: EIP_MEM1.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 9 of 26

EIP FLASH MEMORY ARRAY

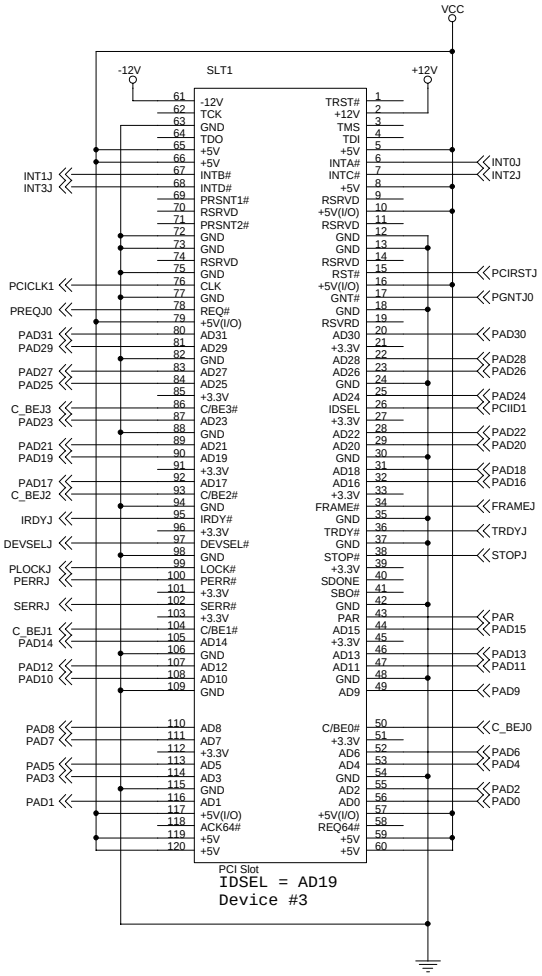


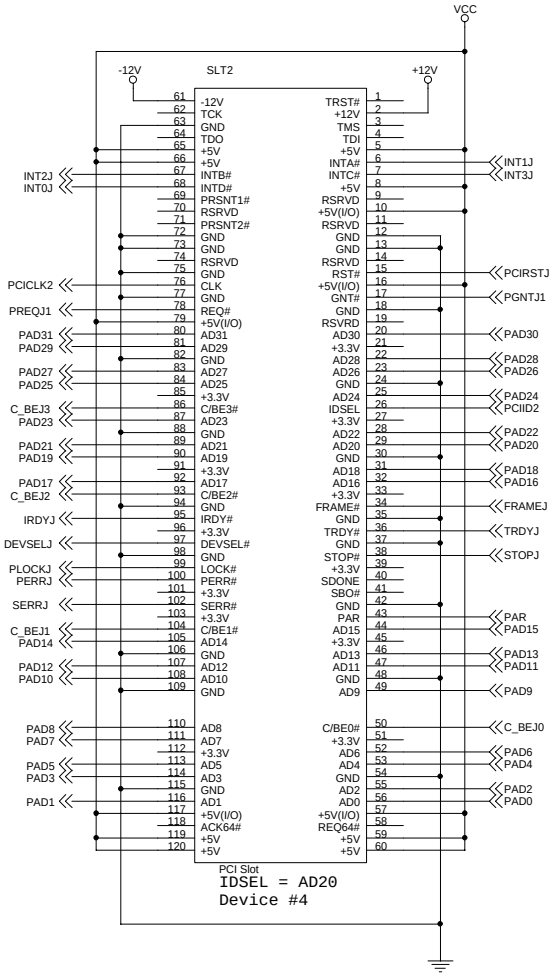
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: EIP_MEM2.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 10 of 26

PCI PULLUPS AND SLOT CONNECTORS; PCI IDSEL GENERATION



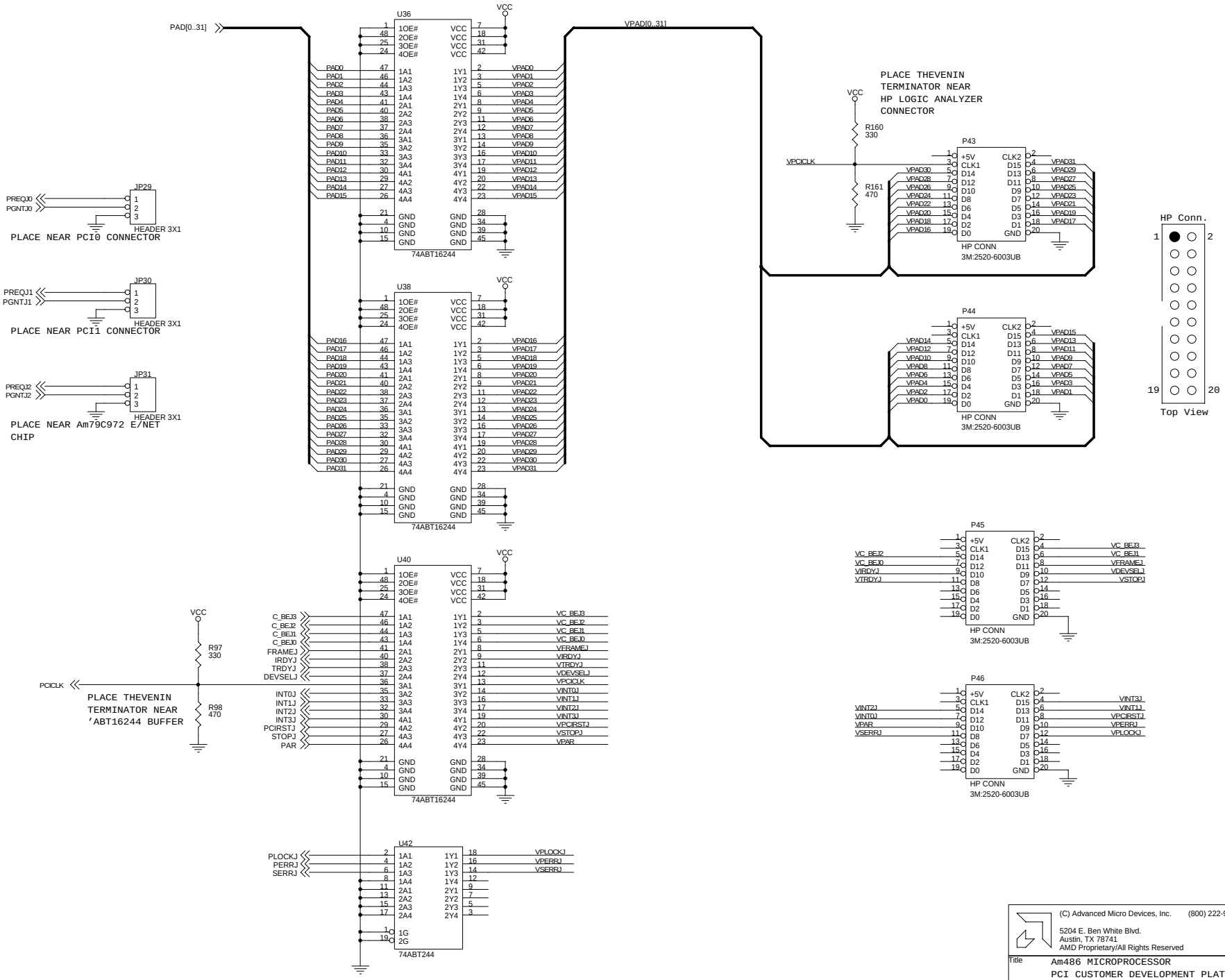
PCIBus INT	Slot1	Slot2	Ethernet
INT0#	INTA#	INTD#	
INT1#	INTB#	INTA#	
INT2#	INTC#	INTB#	INTA#
INT3#	INTC#	INTC#	





Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: PCI_CONN.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 11 of 26

BUFFERS AND LOGIC ANALYZER HEADERS FOR PCI BUS

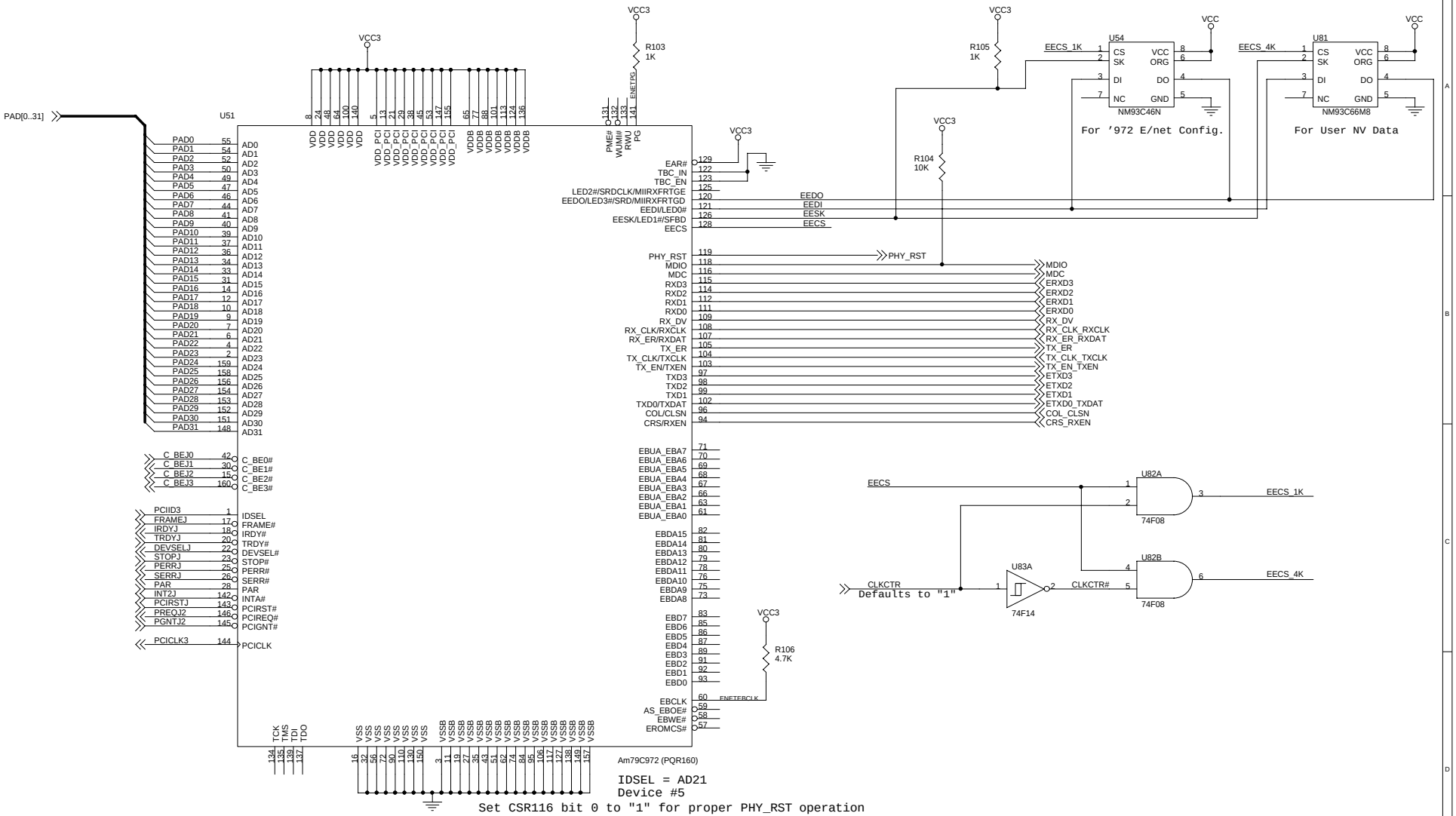


(C) Advanced Micro Devices, Inc. (800) 222-9323

5204 E. Ben White Blvd.
Austin, TX 78741

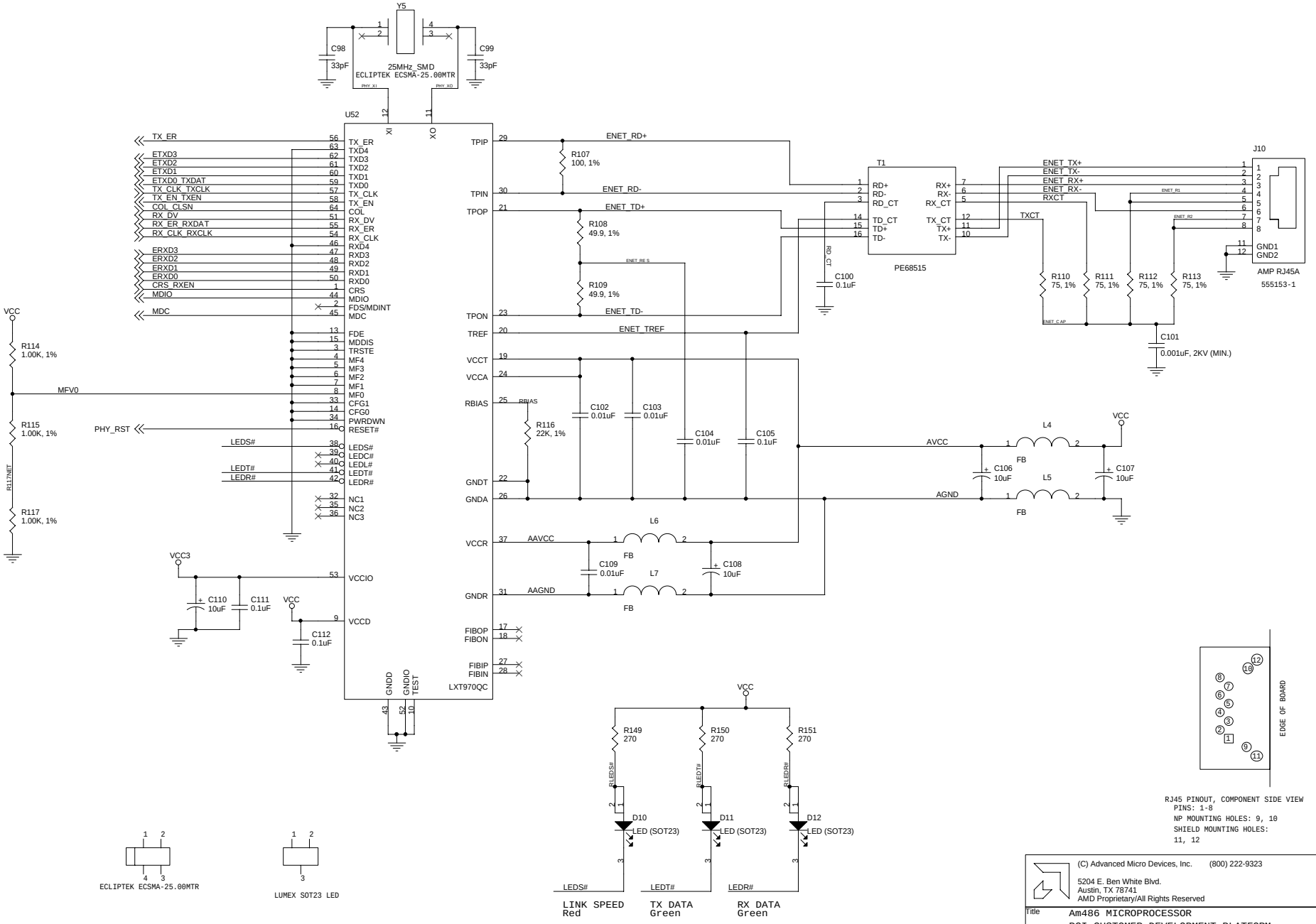
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: PCI_VIS.SCH — Rev: 2.1
Date: Friday, December 04, 1998	Sheet 12 of 26

ETHERNET CONTROLLER, BYPASS CAPACITORS AND POWER SUPPLY FOR ETHERNET CONTROLLER, AND SERIAL EEPROMS



Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: ENET1.SCH — Rev: 2.1
Date: Friday, December 04, 1998	Sheet 13 of 26

ETHERNET PHY CHIP, ETHERNET CONNECTOR, AND LEDS

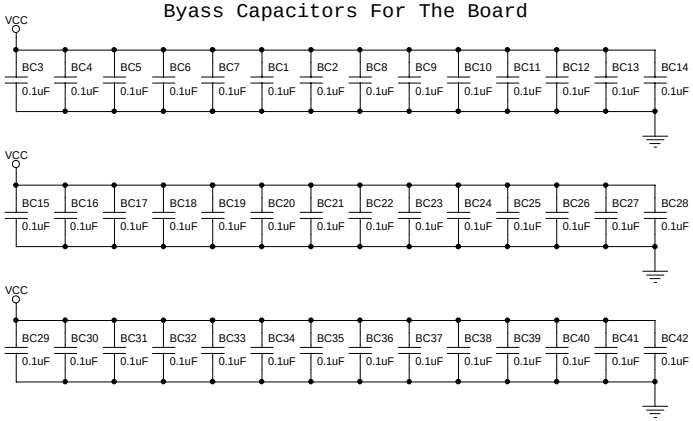


RJ45 PINOUT, COMPONENT SIDE VIEW
PINS: 1-8
NP MOUNTING HOLES: 9, 10
SHIELD MOUNTING HOLES:
11, 12

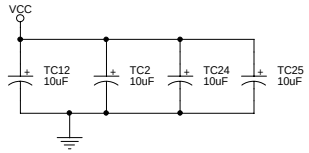
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: ENET2.SCH — Rev: 2.1
Date: Friday, December 04, 1998	Sheet 14 of 26

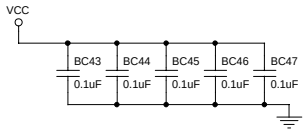
IDE INTERFACE AND BOARD BYPASS CAPACITORS

Byass Capacitors For The Board

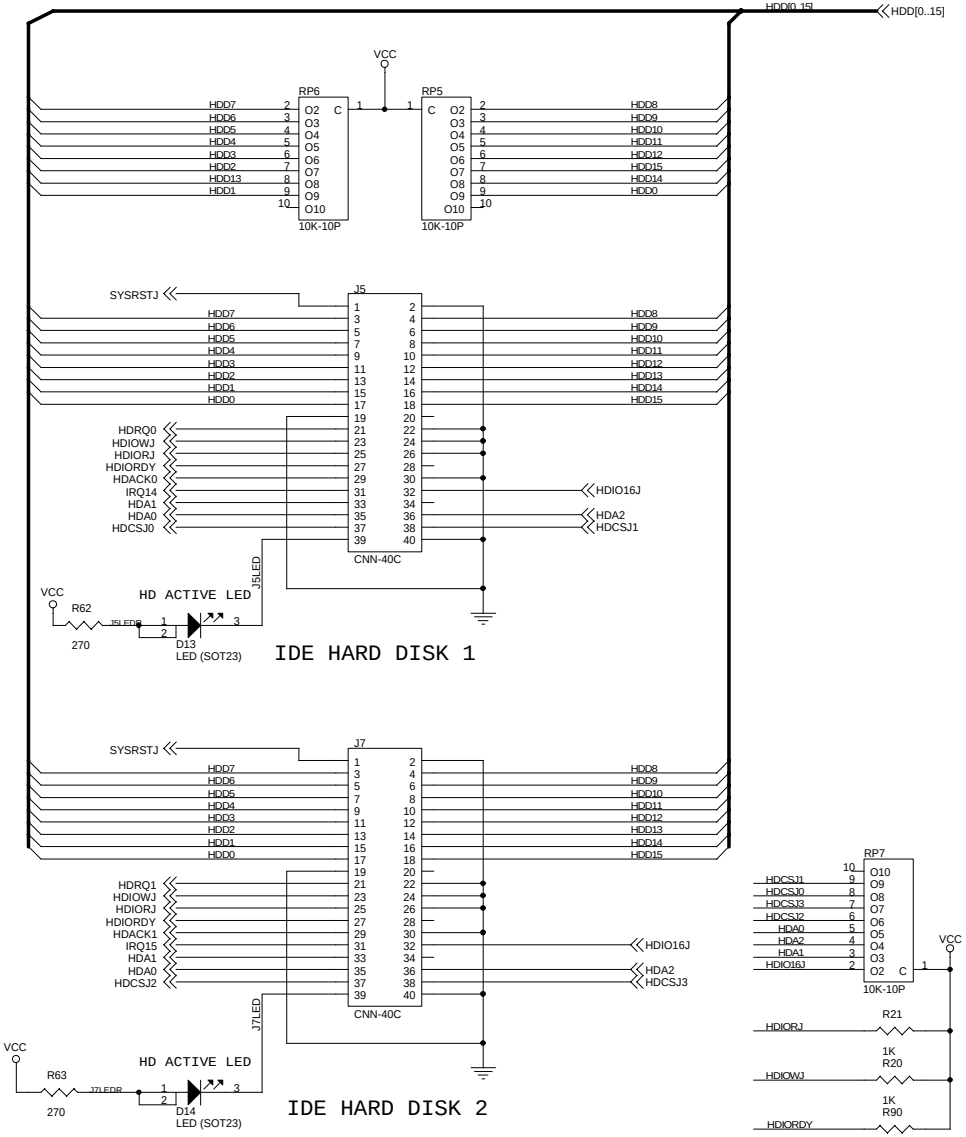


Place one bypass capacitor near each chip Vcc pin, except:
'ABT chips get one on each side near end Vcc pins
QFP chips get one on each side by central Vcc pin

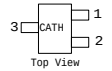




Distribute Tantalum capacitors around the board

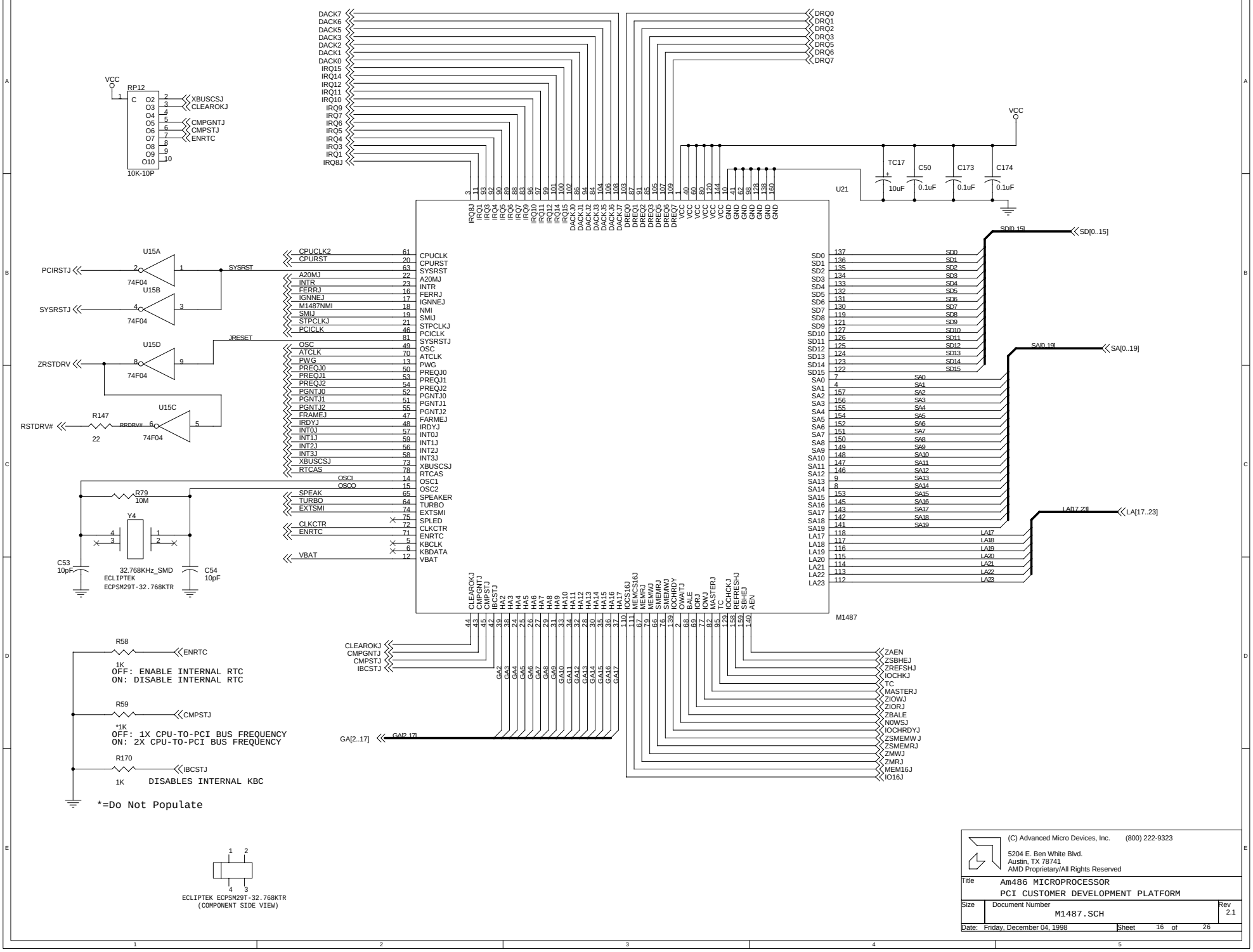


LUMEX LED (SOT23)

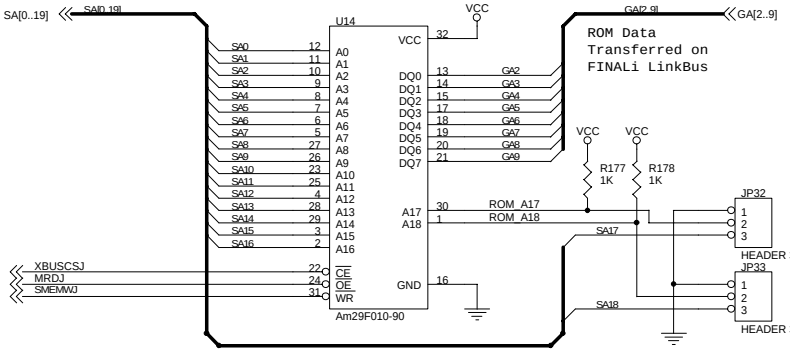


Top View

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: IDE.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 15 of 26

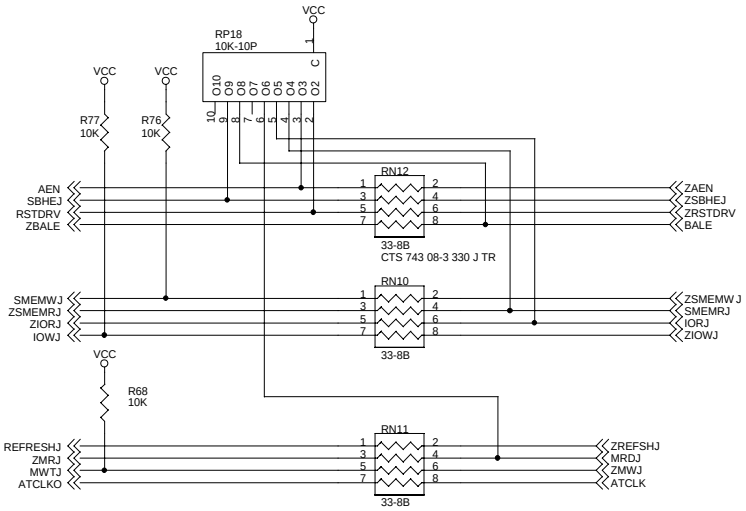

FINALi M1487 INTERFACE
U21
M1487
RP12
10K-10P
XBUSCSJ
CLEAROKJ
CMPGNTJ
CMPSTJ
ENRTC
U15A
U15B
U15C
U15D
74F04
PCIRSTJ
SYSRSTJ
RSTDRV#
ZRSTDRV
SYSRST
JRESET
RRDRV#
R147
22
Y4
32.768KHz_SMD
ECLIPTEK
ECPSM29T-32.768KTR
C53
10pF
C54
10pF
R79
10M
TC17
10uF
C50
0.1uF
C173
0.1uF
C174
0.1uF
VCC
SD[0..15]
SA[0..19]
LA[17..23]
R58
1K
OFF: ENABLE INTERNAL RTC
ON: DISABLE INTERNAL RTC
R59
*1K
OFF: 1X CPU-TO-PCI BUS FREQUENCY
ON: 2X CPU-TO-PCI BUS FREQUENCY
R170
1K
DISABLES INTERNAL KBC
*=Do Not Populate
ECLIPTEK ECPSM29T-32.768KTR
(COMPONENT SIDE VIEW)
(C) Advanced Micro Devices, Inc.
(800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved
Title
Am486 MICROPROCESSOR
PCI CUSTOMER DEVELOPMENT PLATFORM
Size
Document Number
M1487.SCH
Rev
2.1
Date: Friday, December 04, 1998
Sheet 16 of 26

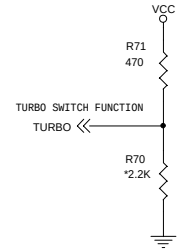
BIOS ROM, ISA SIGNAL SERIES TERMINATION; BATTERY AND SPEAKER CIRCUITS; RESET, SMI, AND NMI PUSHBUTTONS

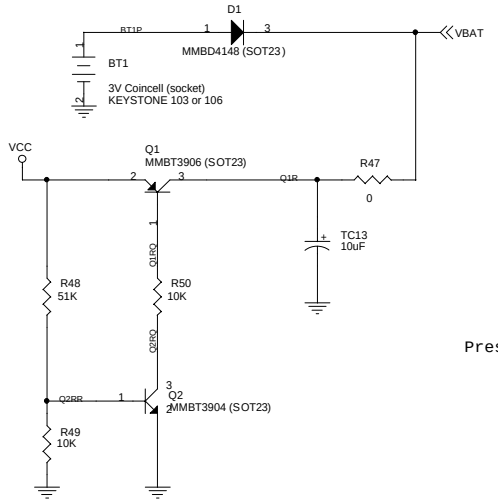


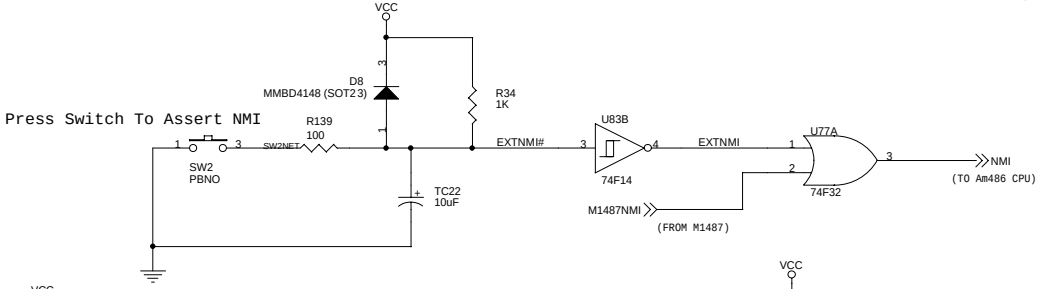
FINALi only supports 1MBit Flash ROM chip (128Kx8 worth of address space) for legacy, desktop PC applications

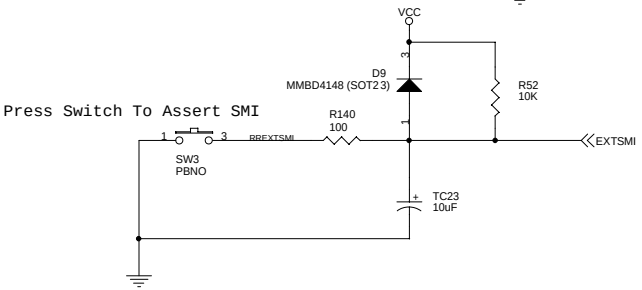
Jumpers to allow multiple 128K BIOS images in the same Flash ROM chip and/or non-PC applications that can use more than 128Kx8 BIOS ROM

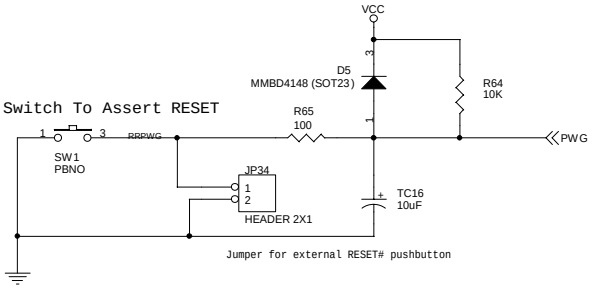


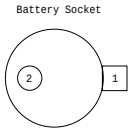


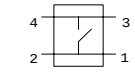


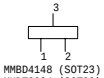


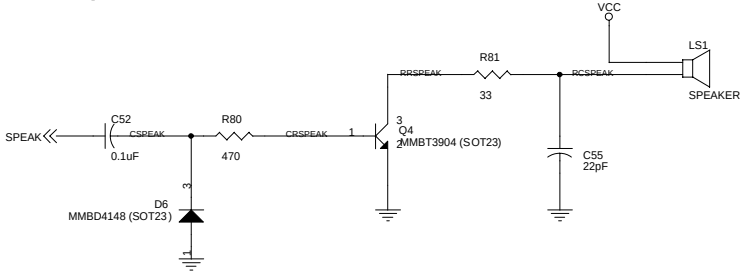


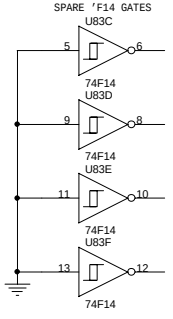






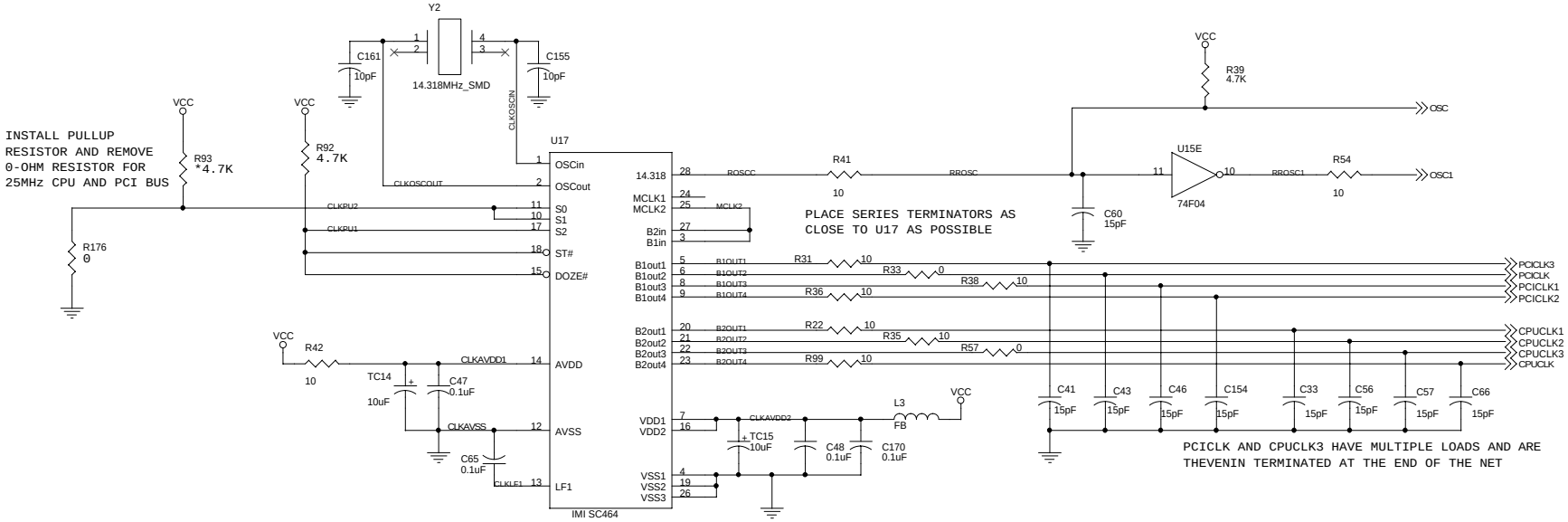


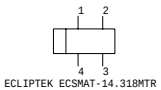




Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: ROM_MISC.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 17 of 26

CLOCK GENERATOR

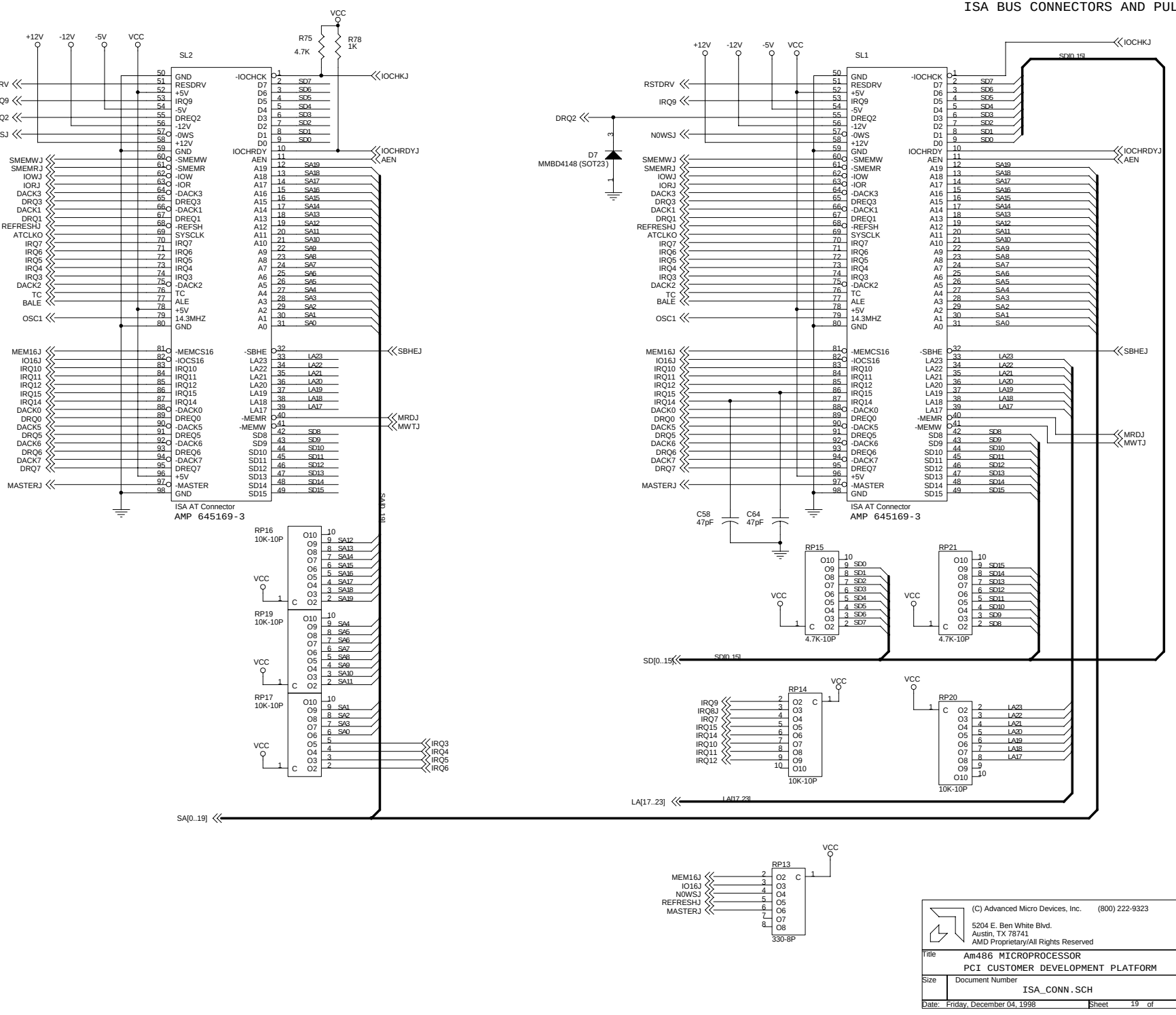




ECLIPTEK ECSMAT-14.318MTR
(COMPONENT SIDE VIEW)

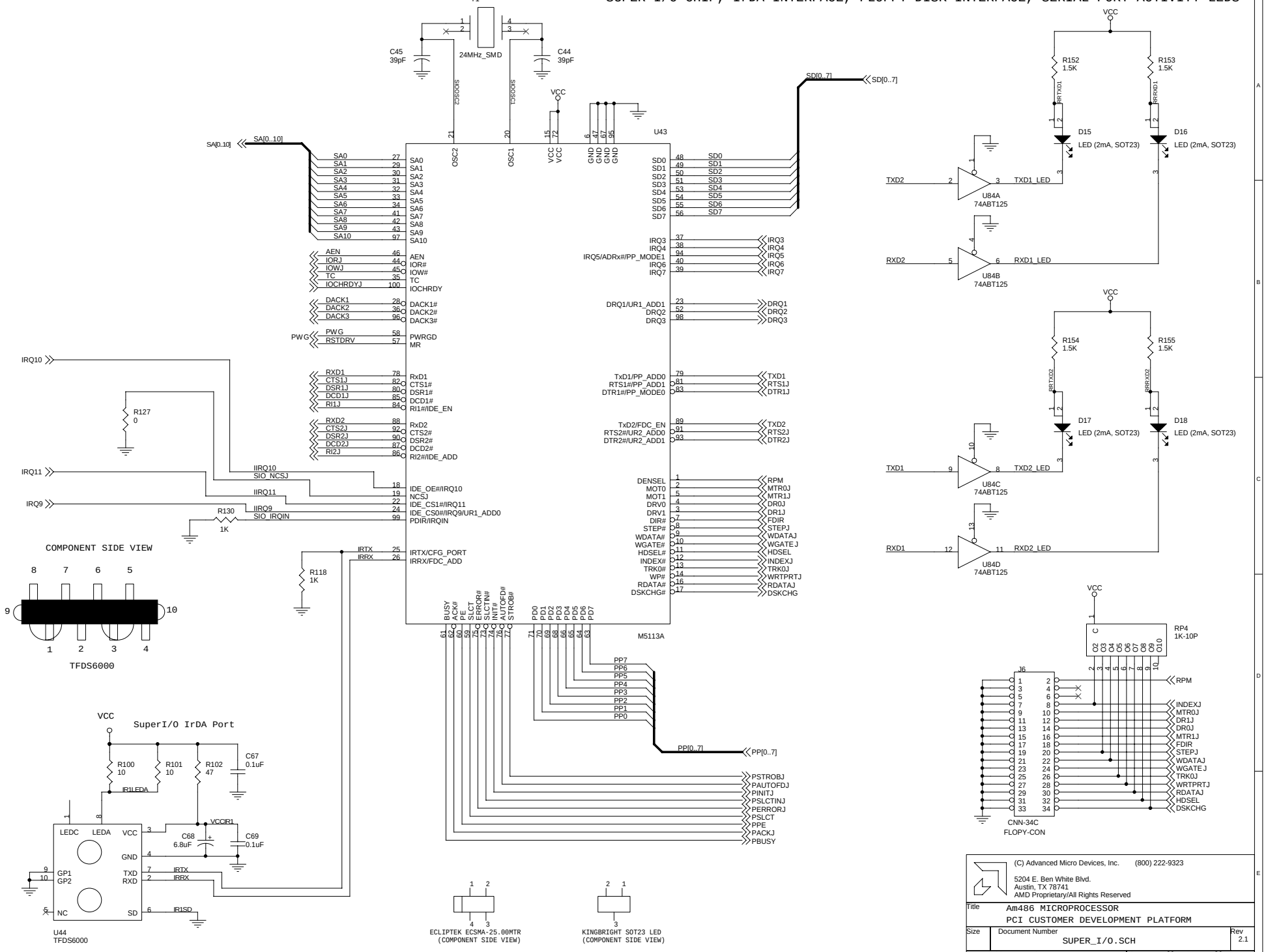
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM	
Size	Document Number CLOCK.SCH	Rev 2.1
Date: Friday, December 04, 1998	Sheet 18 of 26	

ISA BUS CONNECTORS AND PULLUPS



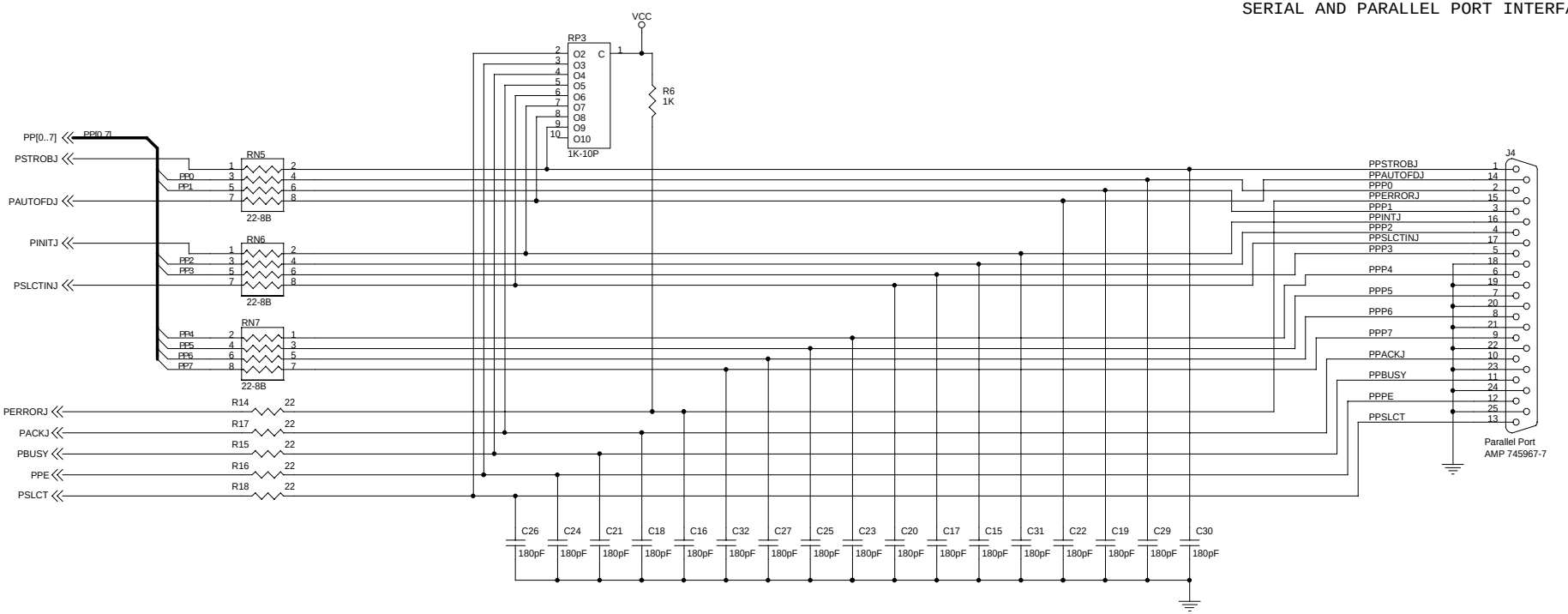
Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: ISA_CONN.SCH — Rev: 2.1
Date: Friday, December 04, 1998	Sheet 19 of 26

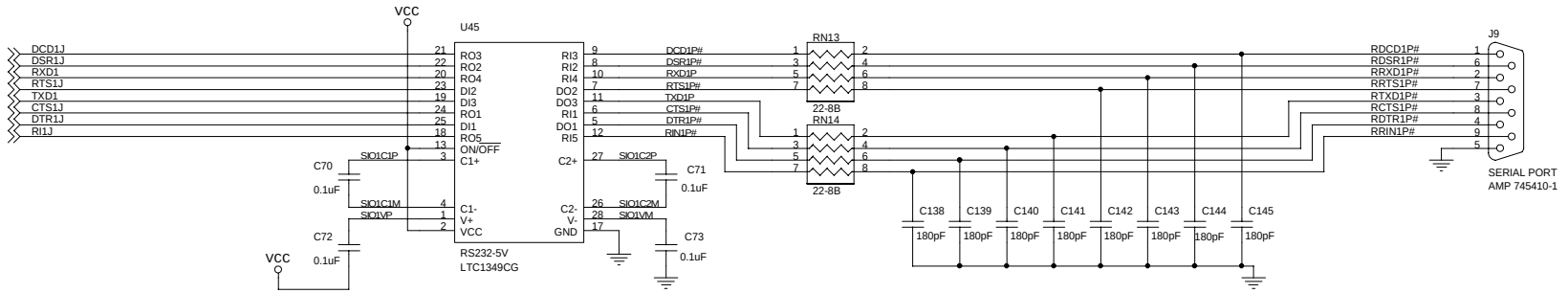
SUPER I/O CHIP, IrDA INTERFACE, FLOPPY DISK INTERFACE, SERIAL PORT ACTIVITY LEDS

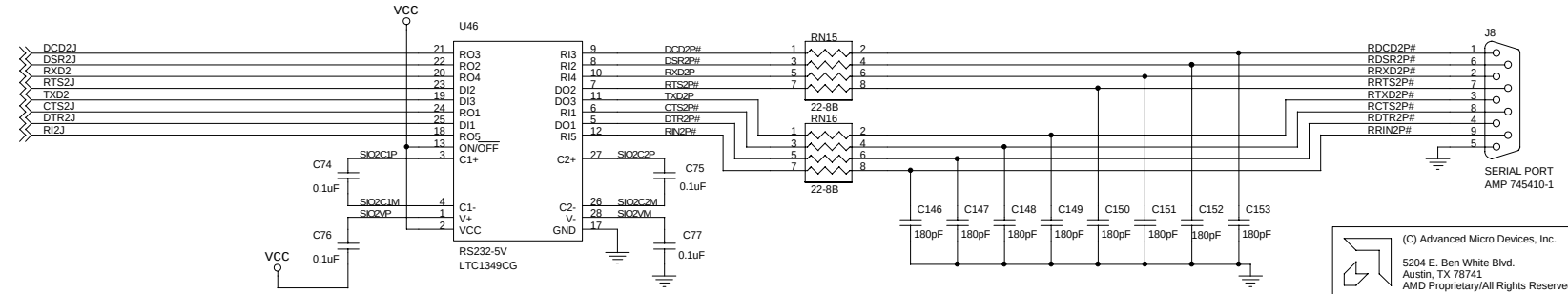


Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: SUPER_I/O.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 20 of 26

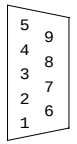
SERIAL AND PARALLEL PORT INTERFACES



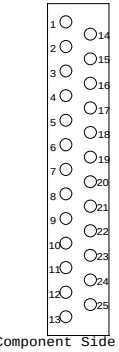




Serial Connector
(Component Side View)



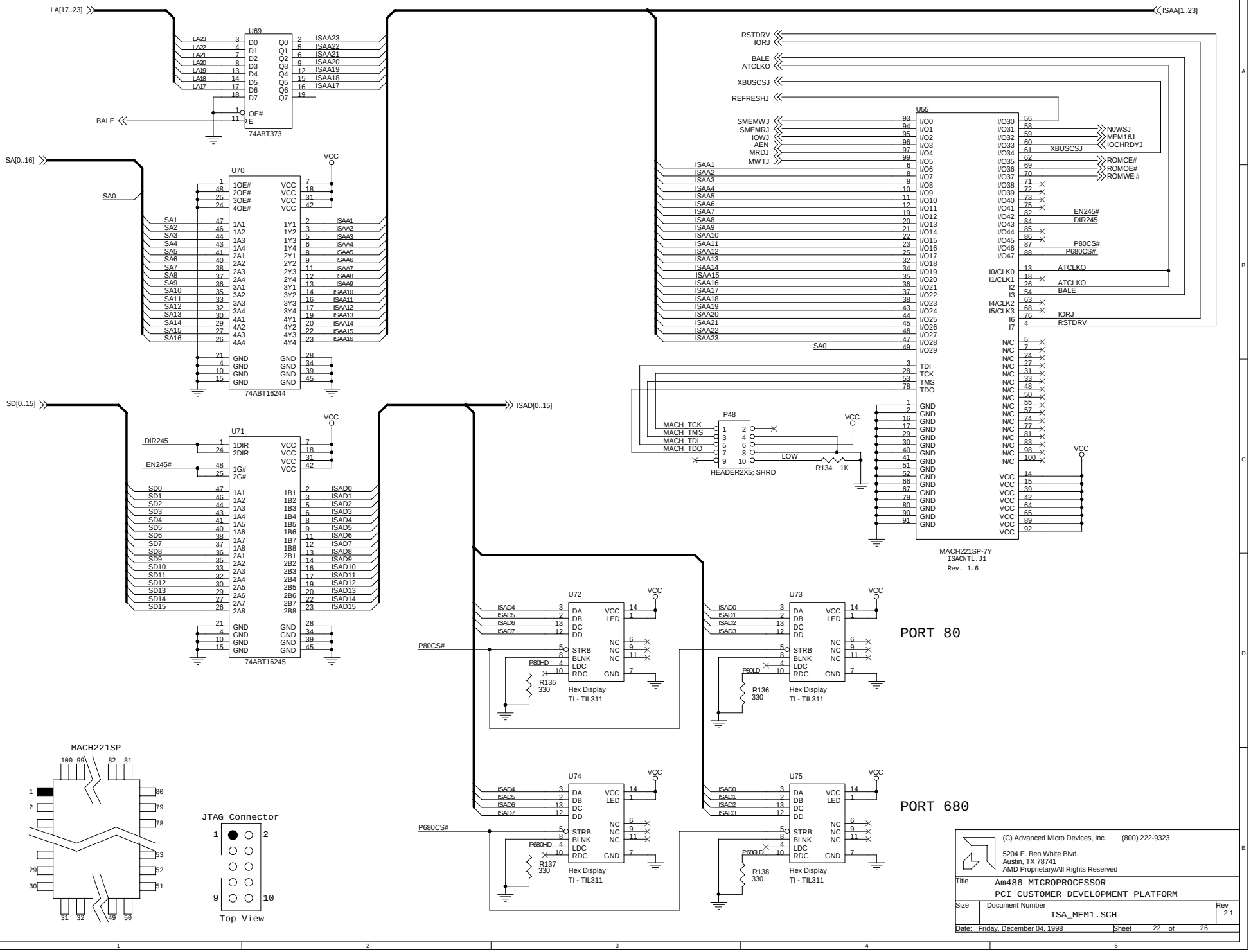
Parallel
Connector



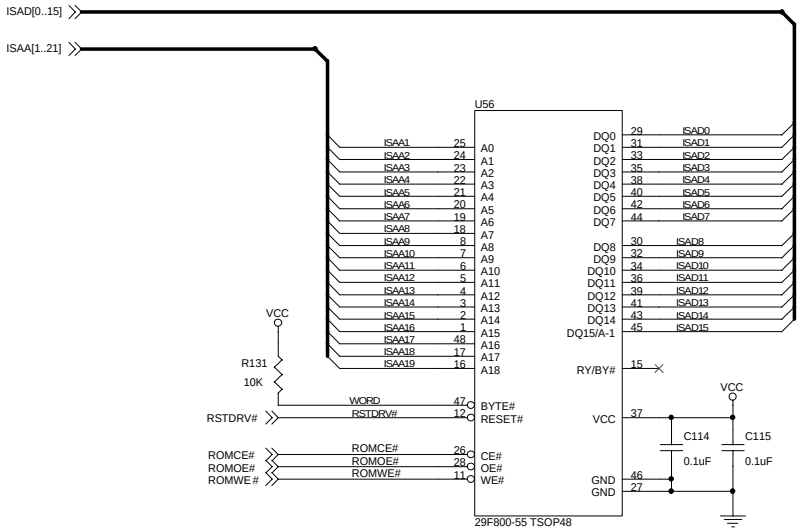
(Component Side View)

Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: SERIAL_PARALLEL.SCH — Rev 2.1
Date: Friday, December 04, 1998	Sheet 21 of 26

INTERFACE FOR ISA BUS MEMORY AND HEX DISPLAYS



Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: ISA_MEM1.SCH — Rev: 2.1
Date: Friday, December 04, 1998	Sheet 22 of 26



1MByte ISA Flash Memory

Configured as 512Kx16bit (29F800T device in "word" mode)

Access at even ISA Memory addresses between 15MB and 16MB-1

Use CSR 12h bit 3 to access 0f00000-0ffffffh as ISA Memory (instead of DRAM, if installed)

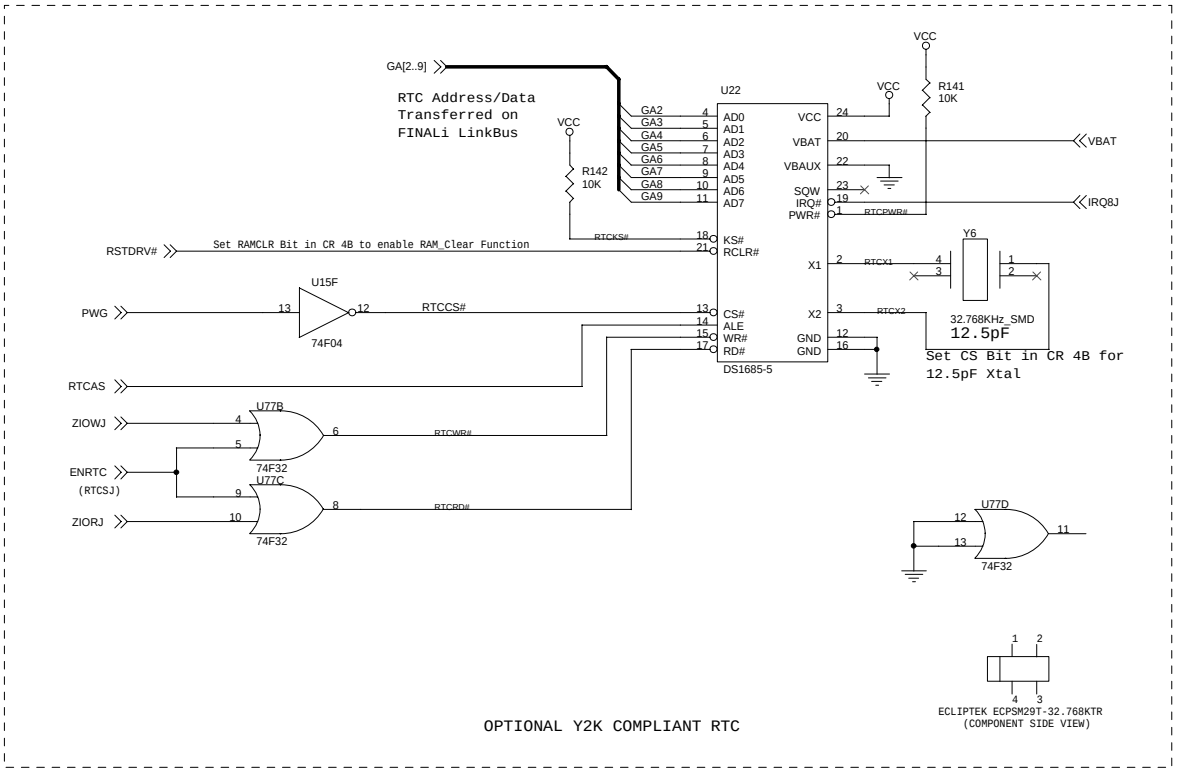
Flash chip A0 pin tied to ISA Address Bit 1; mulitply desired
Flash chip address by 2h to find correct ISA address for access
(ex: Flash chip address 555h is accessed at ISA address AAAh)

Title: Am486 MICROPROCESSOR
PCI CUSTOMER DEVELOPMENT PLATFORM

Size | Document Number: ISA_MEM2.SCH | Rev: 2.1

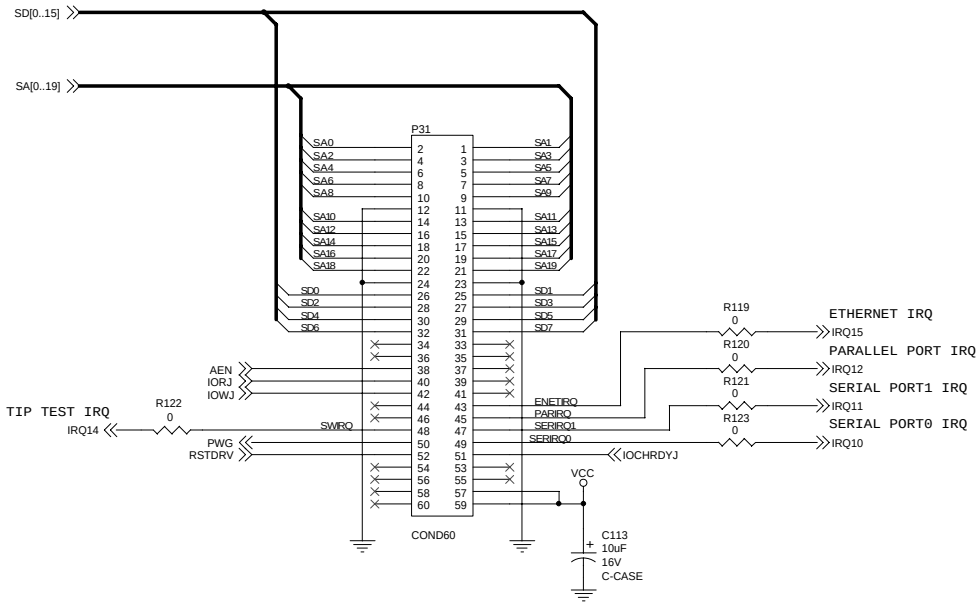
Date: Friday, December 04, 1998 | Sheet 23 of 26

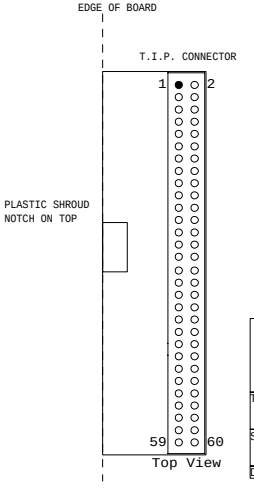
OPTIONAL Y2K RTC AND TEST INTERFACE PORT CONNECTOR



OPTIONAL Y2K COMPLIANT RTC

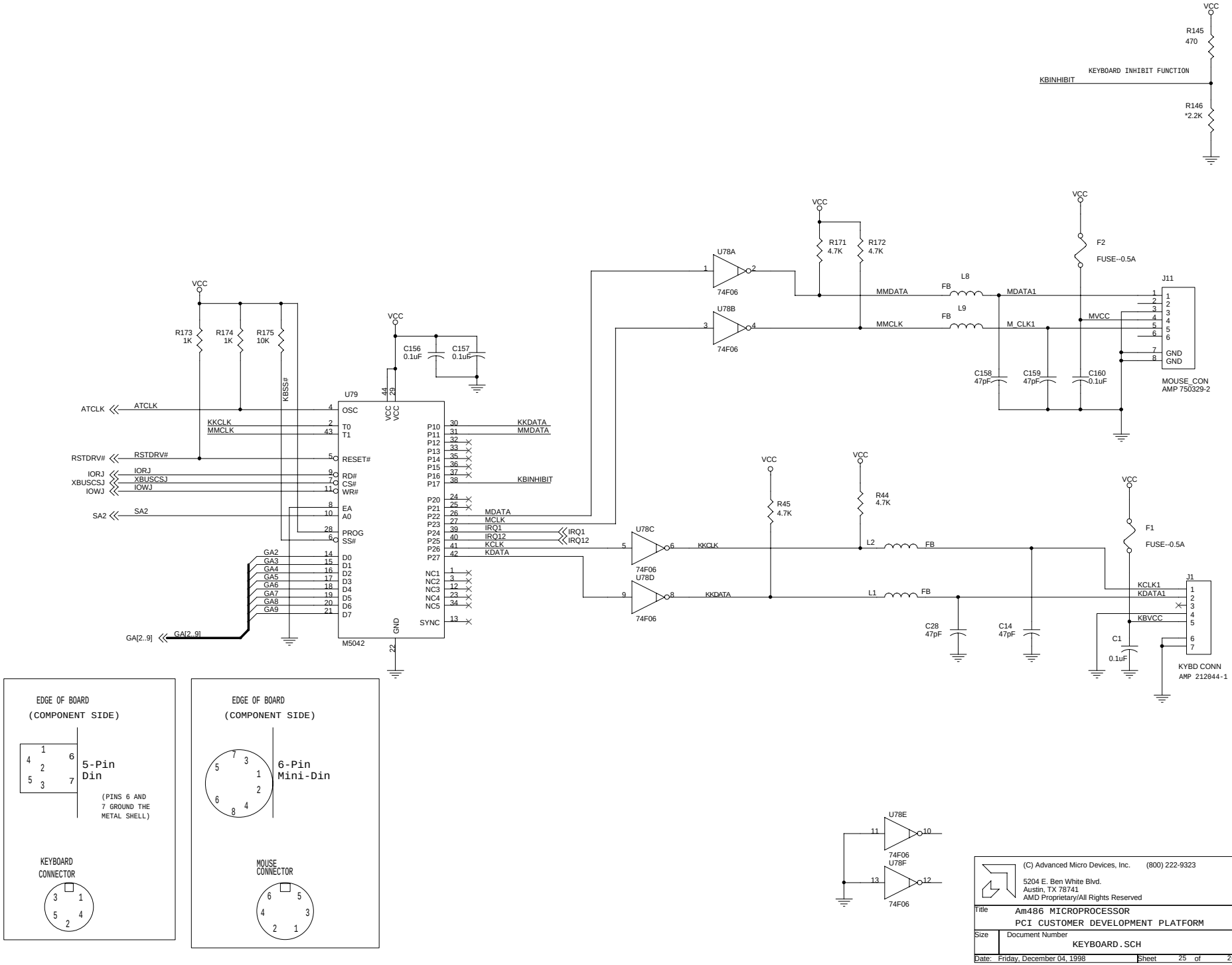
T.I.P. CONNECTOR





Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: RTC_TIP.SCH — Rev: 2.1
Date: Friday, December 04, 1998	Sheet 24 of 26

PC KEYBOARD AND MOUSE INTERFACE

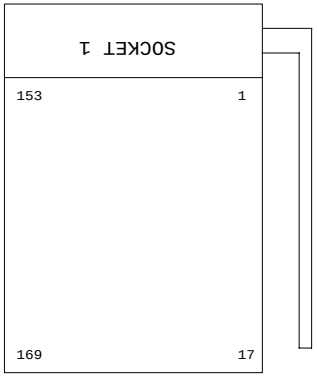


Title	Am486 MICROPROCESSOR PCI CUSTOMER DEVELOPMENT PLATFORM
Size	Document Number: KEYBOARD.SCH — Rev: 2.1
Date: Friday, December 04, 1998	Sheet 25 of 26

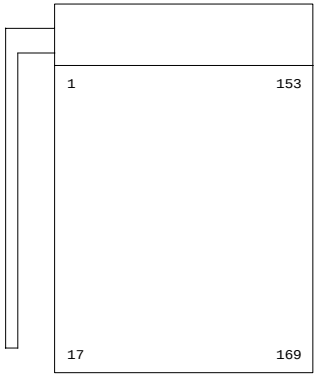
SOCKET1
Am486 MICROPROCESSOR
(PIN #)-PIN DESIGNATION
(PIN SIDE VIEW)

(1)-D20	(18)-D19	(35)-D11	(52)-D9	(59)-GND	(65)-DP1	(71)-GND	(77)-GND	(83)-INC	(89)-GND	(95)-GND	(101)-GND	(107)-D2	(113)-D0	(119)-A31	(136)-A28	(153)-A27
(2)-D22	(19)-D21	(36)-D18	(53)-D13	(60)-VCC	(66)-D8	(72)-VCC	(78)-D3	(84)-D5	(90)-VCC	(96)-D6	(102)-VCC	(108)-D1	(114)-A29	(120)-GND	(137)-A25	(154)-A26
(3)-TCK	(20)-GND	(37)-CLK	(54)-D17	(61)-D10	(67)-D15	(73)-D12	(79)-DP2	(85)-D16	(91)-D14	(97)-D7	(103)-D4	(109)-DP0	(115)-A30	(121)-A17	(138)-VCC	(155)-A23
(4)-D23	(21)-GND	(38)-VCC	(55)-SKT1_NC											(122)-A19	(139)-GND	(156)-VOLDET
(5)-DP3	(22)-GND	(39)-VCC												(123)-A21	(140)-A18	(157)-A14
(6)-D24	(23)-D25	(40)-D27												(124)-A24	(141)-VCC	(158)-GND
(7)-GND	(24)-VCC	(41)-D26												(125)-A22	(142)-A15	(159)-A12
(8)-D29	(25)-D31	(42)-D28												(126)-A20	(143)-VCC	(160)-GND
(9)-GND	(26)-VCC	(43)-D30												(127)-A16	(144)-VCC	(161)-GND
(10)-INV	(27)-SMI#	(44)-SRESET												(128)-A13	(145)-VCC	(162)-GND
(11)-GND	(28)-VCC	(45)-UP#												(129)-A9	(146)-VCC	(163)-GND
(12)-HITM#	(29)-CACHE#	(46)-SMIACT#												(130)-A5	(147)-A11	(164)-GND
(13)-INC	(30)-WB/WT#	(47)-INC												(131)-A7	(148)-A8	(165)-A10
(14)-TDI	(31)-TMS	(48)-FERR#												(132)-A2	(149)-VCC	(166)-GND
(15)-IGNEE#	(32)-NMI	(49)-FLUSH#	(56)-A20M#	(62)-HOLD	(68)-KEN#	(74)-STPCLK#	(80)-BRDY#	(86)-BE2#	(92)-BE0#	(98)-PWT	(104)-D/C#	(110)-LOCK#	(116)-HLDA	(133)-BREQ	(150)-A3	(167)-A6
(16)-INTR	(33)-TDO	(50)-RESET	(57)-BS8#	(63)-VCC	(69)-RDY#	(75)-VCC	(81)-VCC	(87)-BE1#	(93)-VCC	(99)-VCC	(105)-VCC	(111)-M/IO#	(117)-VCC	(134)-PLOCK#	(151)-BLAST#	(168)-A4
(17)-AHOLD	(34)-EADS#	(51)-BS16#	(58)-BOFF#	(64)-GND	(70)-BE3#	(76)-GND	(82)-GND	(88)-PCD	(94)-GND	(100)-GND	(106)-GND	(112)-W/R#	(118)-GND	(135)-PCHK#	(152)-CLKMUL	(169)-ADS#

Am486 MICROPROCESSOR
PIN SIDE VIEW



COMPONENT SIDE VIEW



SOLDER SIDE VIEW

Title: Am486 MICROPROCESSOR
PCI CUSTOMER DEVELOPMENT PLATFORM

Size | Document Number: CPU_PINOUT.SCH | Rev: 2.1

Date: Friday, December 04, 1998 | Sheet 26 of 26