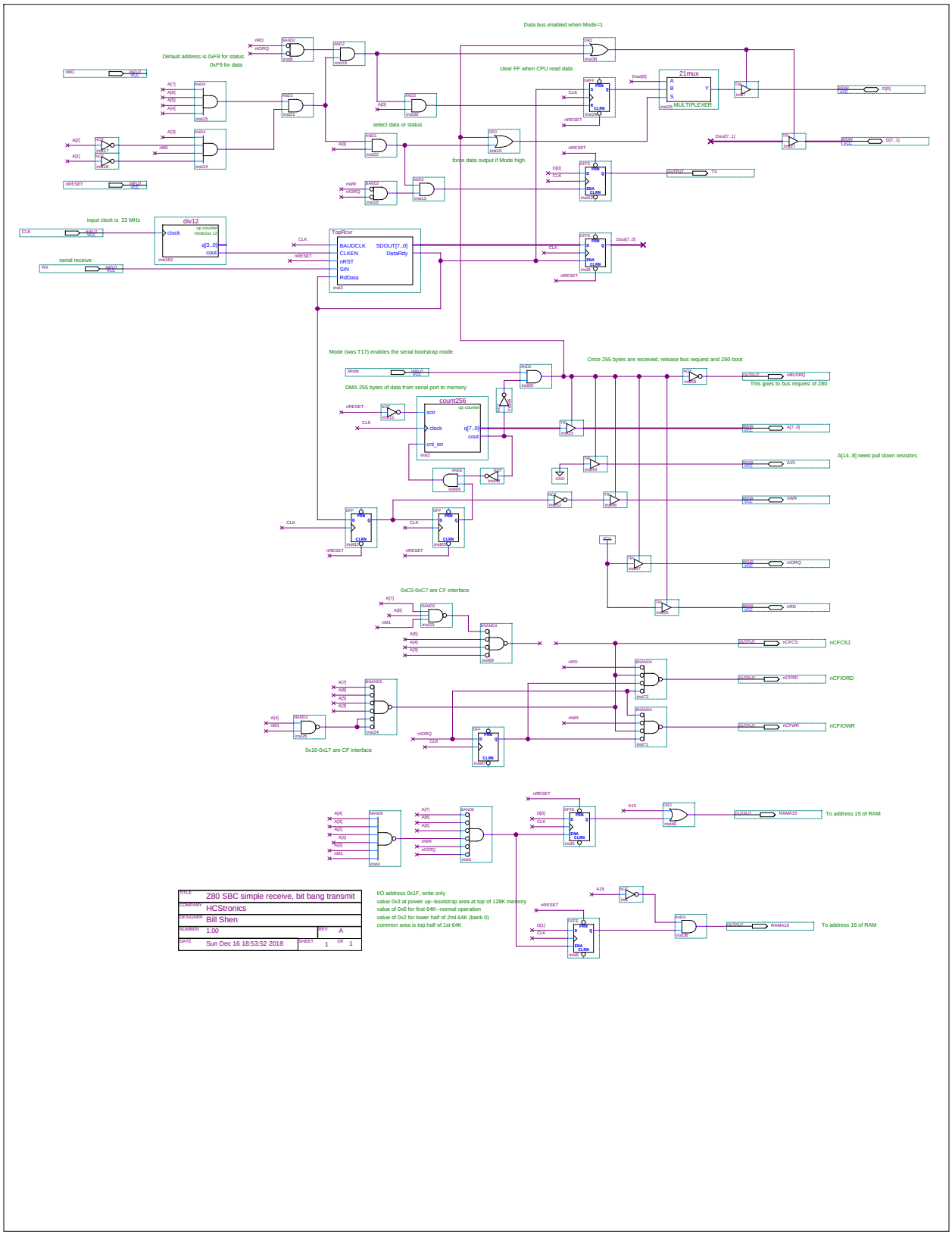
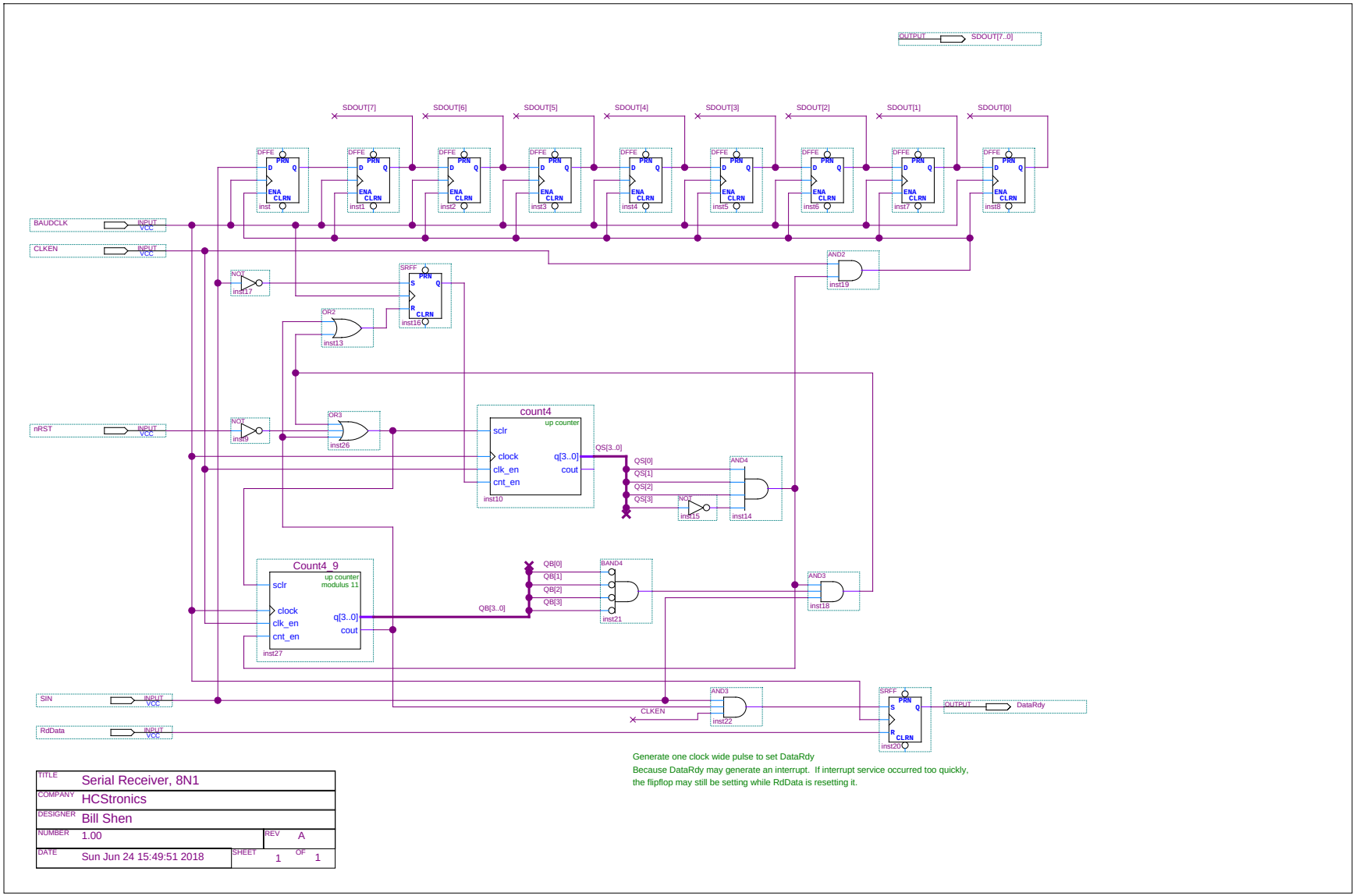

Data bus enabled when Mode=1
Default address is 0xF8 for status
0xF9 for data
clear FF when CPU read data
select data or status
force data output if Mode high
21mux
MULTIPLEXER
input clock is 22 MHz
div12
TopRcvr
BAUDCLK
CLKEN
nRST
SIN
RdData
SDOUT[7..0]
DataRdy
serial receive
Mode (was T17) enables the serial bootstrap mode
Once 255 bytes are received, release bus request and Z80 boot
This goes to bus request of Z80
DMA 255 bytes of data from serial port to memory
count256
A(14..8) need pull down resistors
0xC0-0xC7 are CF interface
0x10-0x17 are CF interface
nCFCS1
nCFIORD
nCFIOWR
To address 15 of RAM
To address 16 of RAM
I/O address 0x1F, write only
value 0x3 at power up--bootstrap area at top of 128K memory
value of 0x0 for first 64K--normal operation
value of 0x2 for lower half of 2nd 64K (bank 0)
common area is top half of 1st 64K
TITLE Z80 SBC simple receive, bit bang transmit
COMPANY HCStronics
DESIGNER Bill Shen
NUMBER 1.00
REV A
DATE Sun Dec 16 18:53:52 2018
SHEET 1 OF 1


SDOUT[7..0]
SDOUT[7]
SDOUT[6]
SDOUT[5]
SDOUT[4]
SDOUT[3]
SDOUT[2]
SDOUT[1]
SDOUT[0]
BAUDCLK
CLKEN
nRST
SIN
RdData
count4
up counter
sclr
clock
clk_en
cnt_en
q[3..0]
cout
QS[3..0]
QS[0]
QS[1]
QS[2]
QS[3]
Count4_9
up counter
modulus 11
QB[3..0]
QB[0]
QB[1]
QB[2]
QB[3]
CLKEN
DataRdy
Generate one clock wide pulse to set DataRdy
Because DataRdy may generate an interrupt. If interrupt service occurred too quickly,
the flipflop may still be setting while RdData is resetting it.
TITLE Serial Receiver, 8N1
COMPANY HCStronics
DESIGNER Bill Shen
NUMBER 1.00
REV A
DATE Sun Jun 24 15:49:51 2018
SHEET 1 OF 1