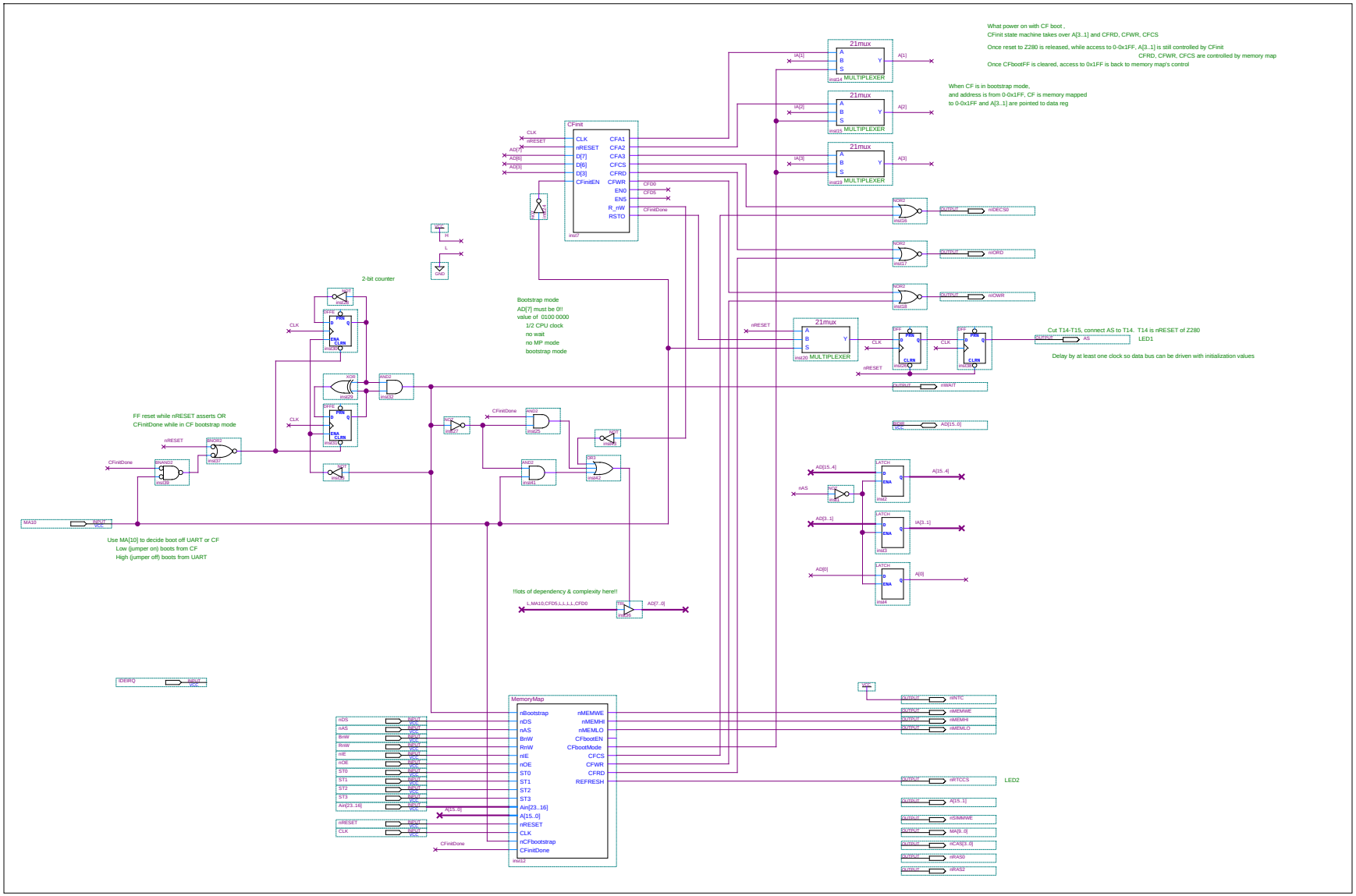
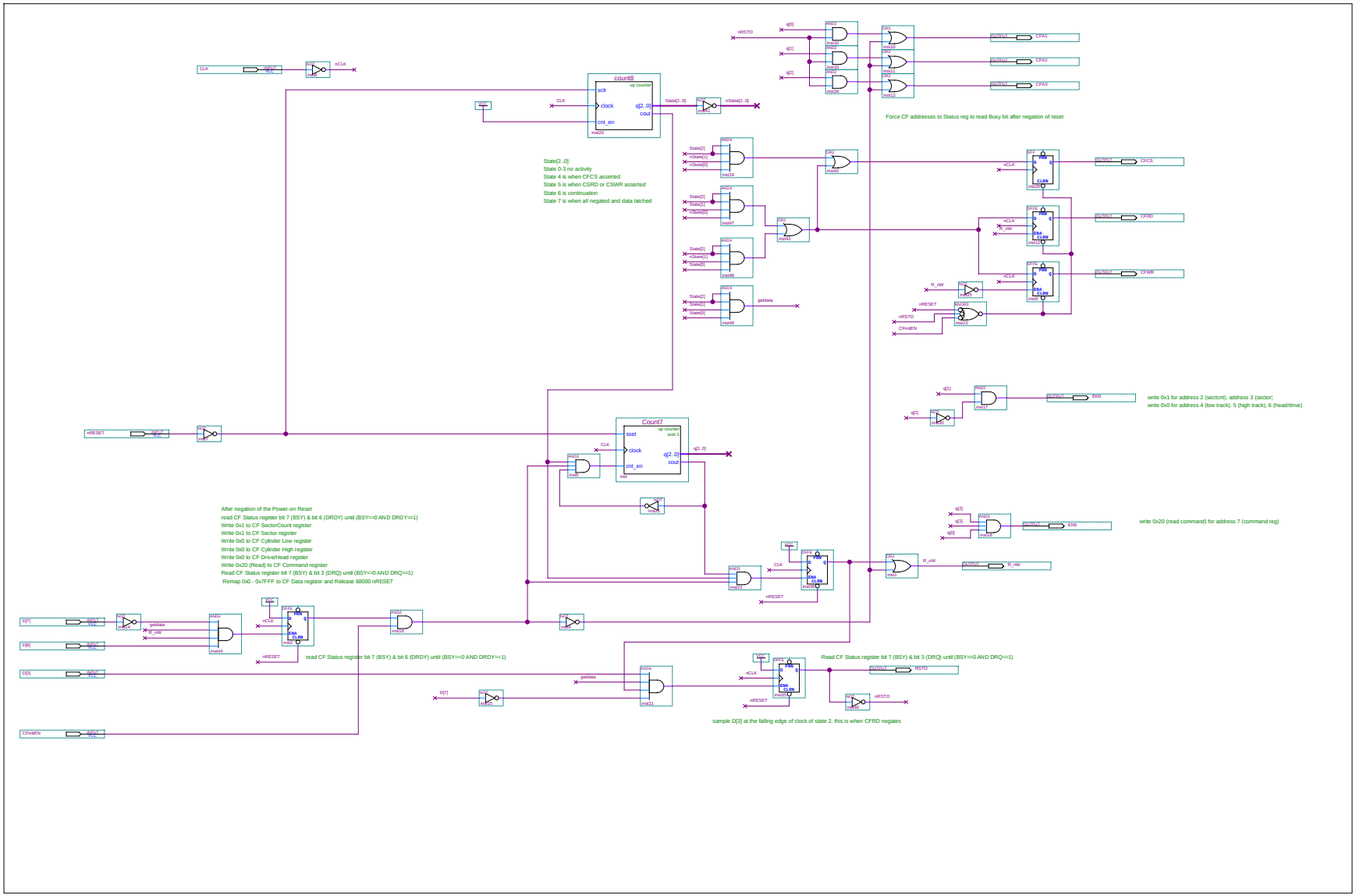
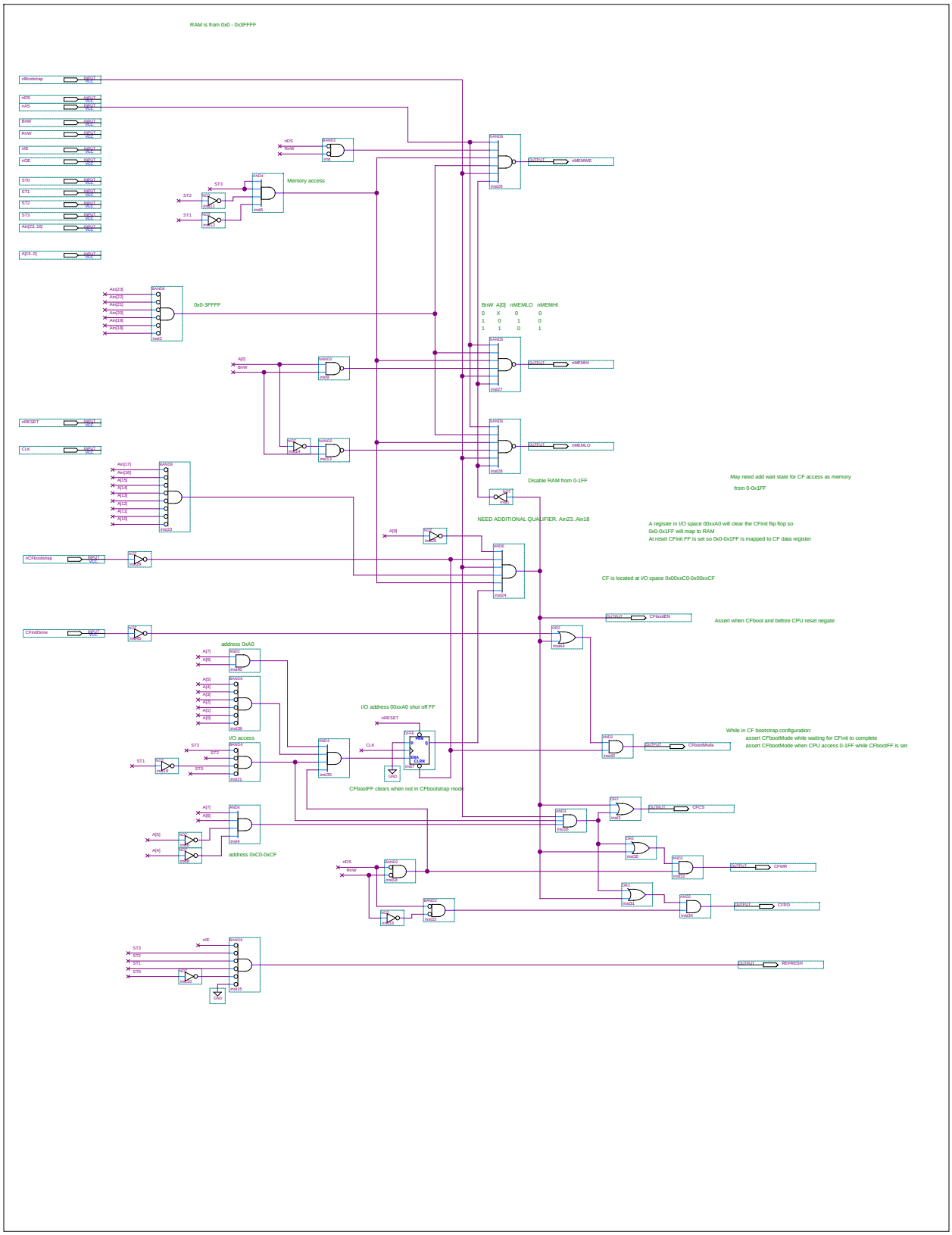

What power on with CF boot ,
CFinit state machine takes over A[3..1] and CFRD, CFWR, CFCS
Once reset to Z280 is released, while access to 0-0x1FF, A[3..1] is still controlled by CFinit
CFRD, CFWR, CFCS are controlled by memory map
Once CFbootFF is cleared, access to 0x1FF is back to memory map's control
When CF is in bootstrap mode,
and address is from 0-0x1FF, CF is memory mapped
to 0-0x1FF and A[3..1] are pointed to data reg
21mux
MULTIPLEXER
CFinit
CLK
nRESET
D[7]
D[6]
D[3]
CFinitEN
CFA1
CFA2
CFA3
CFCS
CFRD
CFWR
EN0
EN5
R_nW
RSTO
CFD0
CFD5
CFinitDone
2-bit counter
Bootstrap mode
AD[7] must be 0!!
value of 0100 0000
1/2 CPU clock
no wait
no MP mode
bootstrap mode
nIDECS0
nIORD
nIOWR
nWAIT
AD[15..0]
Cut T14-T15, connect AS to T14. T14 is nRESET of Z280
LED1
Delay by at least one clock so data bus can be driven with initialization values
FF reset while nRESET asserts OR
CFinitDone while in CF bootstrap mode
MA10
Use MA[10] to decide boot off UART or CF
Low (jumper on) boots from CF
High (jumper off) boots from UART
!!lots of dependency & complexity here!!
L,MA10,CFD5,L,L,L,L,CFD0
AD[7..0]
IDEIRQ
MemoryMap
nBootstrap
nDS
nAS
BnW
RnW
nIE
nOE
ST0
ST1
ST2
ST3
Ain[23..16]
A[15..0]
nRESET
CLK
nCFbootstrap
CFinitDone
nMEMWE
nMEMHI
nMEMLO
CFbootEN
CFbootMode
CFCS
CFWR
CFRD
REFRESH
nINTC
nMEMWE
nMEMHI
nMEMLO
nRTCCS
LED2
A[15..1]
nSIMMWE
MA[9..0]
nCAS[3..0]
nRAS0
nRAS2


CLK
nCLK
nRESET
CFinitEN
count8
up counter
sclr
clock
cnt_en
q[2..0]
cout
State[2..0]
nState[2..0]
State[2..0]:
State 0-3 no activity
State 4 is when CFCS asserted
State 5 is when CSRD or CSWR asserted
State 6 is continuation
State 7 is when all negated and data latched
getdata
Force CF addresses to Status reg to read Busy bit after negation of reset
CFA1
CFA2
CFA3
CFCS
CFRD
CFWR
ENB
write 0x1 for address 2 (sectcnt), address 3 (sector)
write 0x0 for address 4 (low track), 5 (high track), 6 (head/drive)
Count7
sset
sset 1
After negation of the Power-on Reset
read CF Status register bit 7 (BSY) & bit 6 (DRDY) until (BSY==0 AND DRDY==1)
Write 0x1 to CF SectorCount register
Write 0x1 to CF Sector register
Write 0x0 to CF Cylinder Low register
Write 0x0 to CF Cylinder High register
Write 0x0 to CF Drive/Head register
Write 0x20 (Read) to CF Command register
Read CF Status register bit 7 (BSY) & bit 3 (DRQ) until (BSY==0 AND DRQ==1)
Remap 0x0 - 0x7FFF to CF Data register and Release 68000 nRESET
write 0x20 (read command) for address 7 (command reg)
D[7]
D[8]
D[0]
R_nW
read CF Status register bit 7 (BSY) & bit 6 (DRDY) until (BSY==0 AND DRDY==1)
Read CF Status register bit 7 (BSY) & bit 3 (DRQ) until (BSY==0 AND DRQ==1)
BSYO
nRSTO
sample D[3] at the falling edge of clock of state 2, this is when CFRD negates


RAM is from 0x0 - 0x3FFFF
Memory access
0x0-3FFFF
BnW A[0] nMEMLO nMEMHI
0 X 0 0
1 0 1 0
1 1 0 1
Disable RAM from 0-1FF
May need add wait state for CF access as memory
from 0-0x1FF
NEED ADDITIONAL QUALIFIER, Ain23..Ain18
A register in I/O space 00xxA0 will clear the CFinit flip flop so
0x0-0x1FF will map to RAM
At reset CFinit FF is set so 0x0-0x1FF is mapped to CF data register
CF is located at I/O space 0x00xxC0-0x00xxCF
Assert when CFboot and before CPU reset negate
address 0xA0
I/O address 00xxA0 shut off FF
I/O access
While in CF bootstrap configuration:
assert CFbootMode while waiting for CFinit to complete
assert CFbootMode when CPU access 0-1FF while CFbootFF is set
CFbootFF clears when not in CFbootstrap mode
address 0xC0-0xCF