A24 decides whether it is DRAM or flash/RAM/DUART
DRAM base is 1000000
flash base is 0
RAM base is 100000
DUART base is 400000
DRAM base is 1000000

Instrumentation:

ByteDecode

Count32
RF1: latch in the output of refresh timer, waiting for negation of AS
RF2: start of the refresh cycle
RF2.5: CAS asserts at the falling edge of clock
RF3: RAS asserts for 2 clocks

make sure there are enough time for RAS precharge after the refresh is done
hold off clkack until refresh finished
start the refresh when nAS is high
nENCASA, delay by half clock to avoid contention
high if not CAS-before-RAS
Low during CAS-before-RAS when
high when CAS-before-RAS finished
Push RAS out by half clock
So RAS address can stabilize
nENRASA
negate nENRASA
Push RAS out by half clock
So RAS address can stabilize
2 wait states
A24 decides whether it is DRAM or flash/RAM/DUART
flash base is 0
RAM base is 100000
DUART base is 400000
DRAM base is 1000000