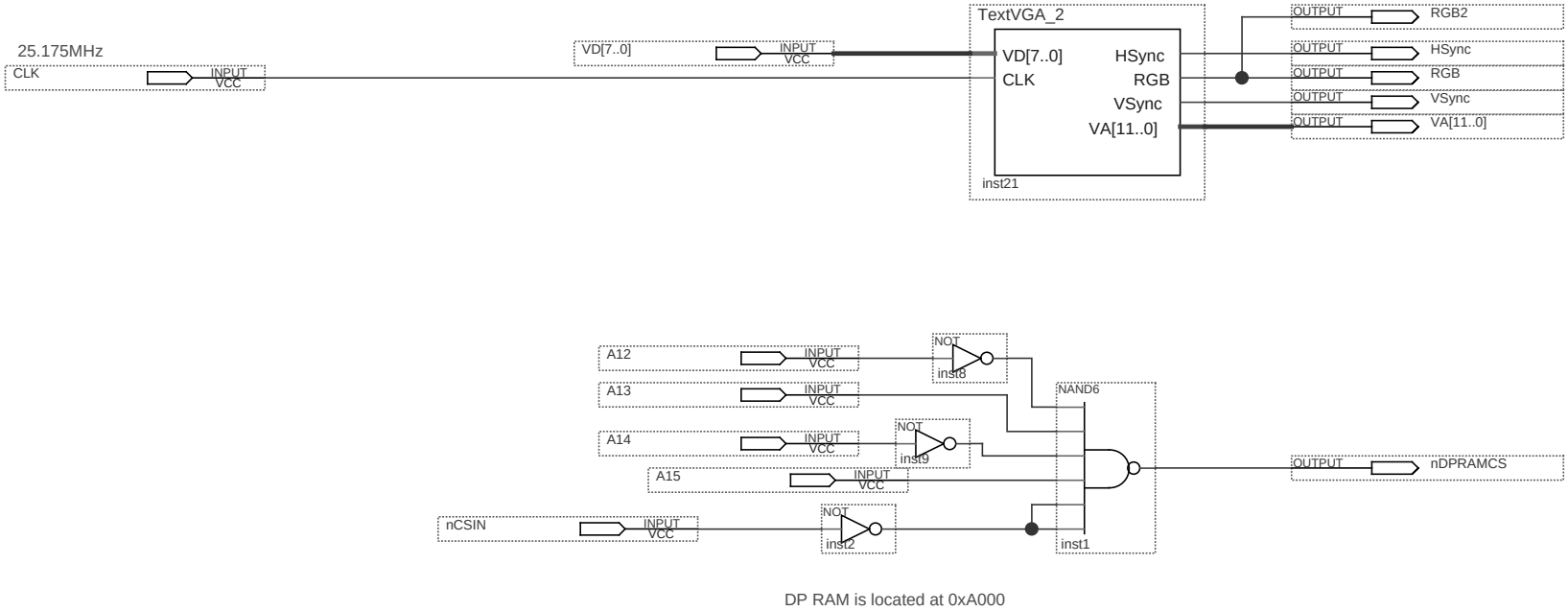
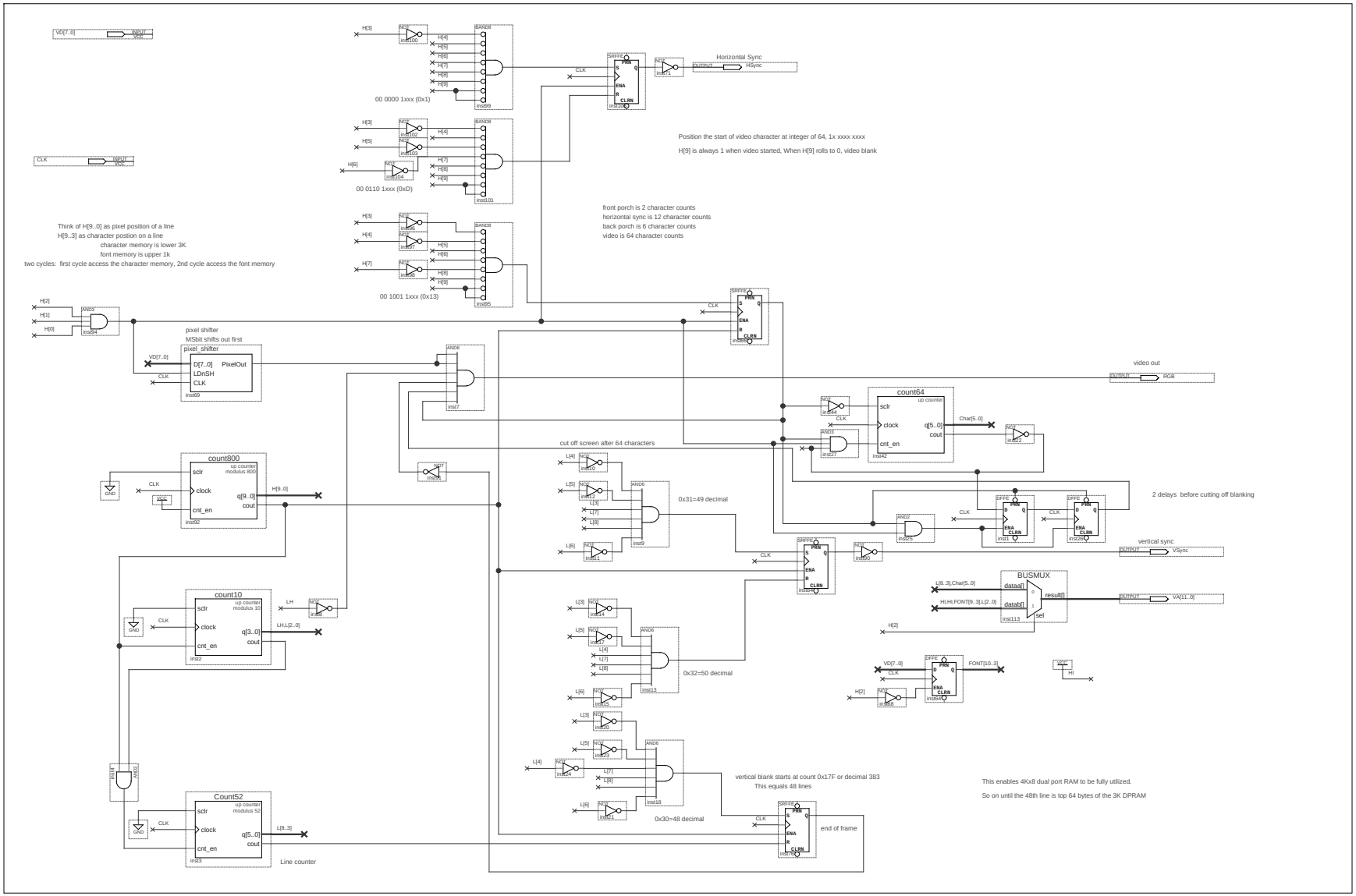


DP RAM is located at 0xA000

TITLE	Piggyback VGA		
COMPANY	HCSTronics		
DESIGNER	Bill Shen		
NUMBER	1.00	REV	A
DATE	Fri May 28 12:43:54 2021	SHEET 1	OF 1


VD[7..0]
CLK
00 0000 1xxx (0x1)
00 0110 1xxx (0xD)
00 1001 1xxx (0x13)
Horizontal Sync
HSync
Position the start of video character at integer of 64, 1x xxxx xxxx
H[9] is always 1 when video started, When H[9] rolls to 0, video blank
front porch is 2 character counts
horizontal sync is 12 character counts
back porch is 6 character counts
video is 64 character counts
Think of H[9..0] as pixel position of a line
H[9..3] as character position on a line
character memory is lower 3K
font memory is upper 1k
two cycles: first cycle access the character memory, 2nd cycle access the font memory
pixel shifter
MSbit shifts out first
pixel_shifter
D[7..0]
PixelOut
LDnSH
video out
RGB
count64
up counter
sclr
clock
cnt_en
q[5..0]
cout
Char[5..0]
cut off screen after 64 characters
count800
q[9..0]
H[9..0]
0x31=49 decimal
2 delays before cutting off blanking
vertical sync
VSync
BUSMUX
dataa[]
datab[]
result[]
sel
VA[11..0]
count10
modulus 10
q[3..0]
LH
LH,L[2..0]
0x32=50 decimal
FONT[10..3]
Hi
Count52
modulus 52
q[5..0]
L[8..3]
Line counter
0x30=48 decimal
vertical blank starts at count 0x17F or decimal 383
This equals 48 lines
end of frame
This enables 4Kx8 dual port RAM to be fully utilized.
So on until the 48th line is top 64 bytes of the 3K DPRAM