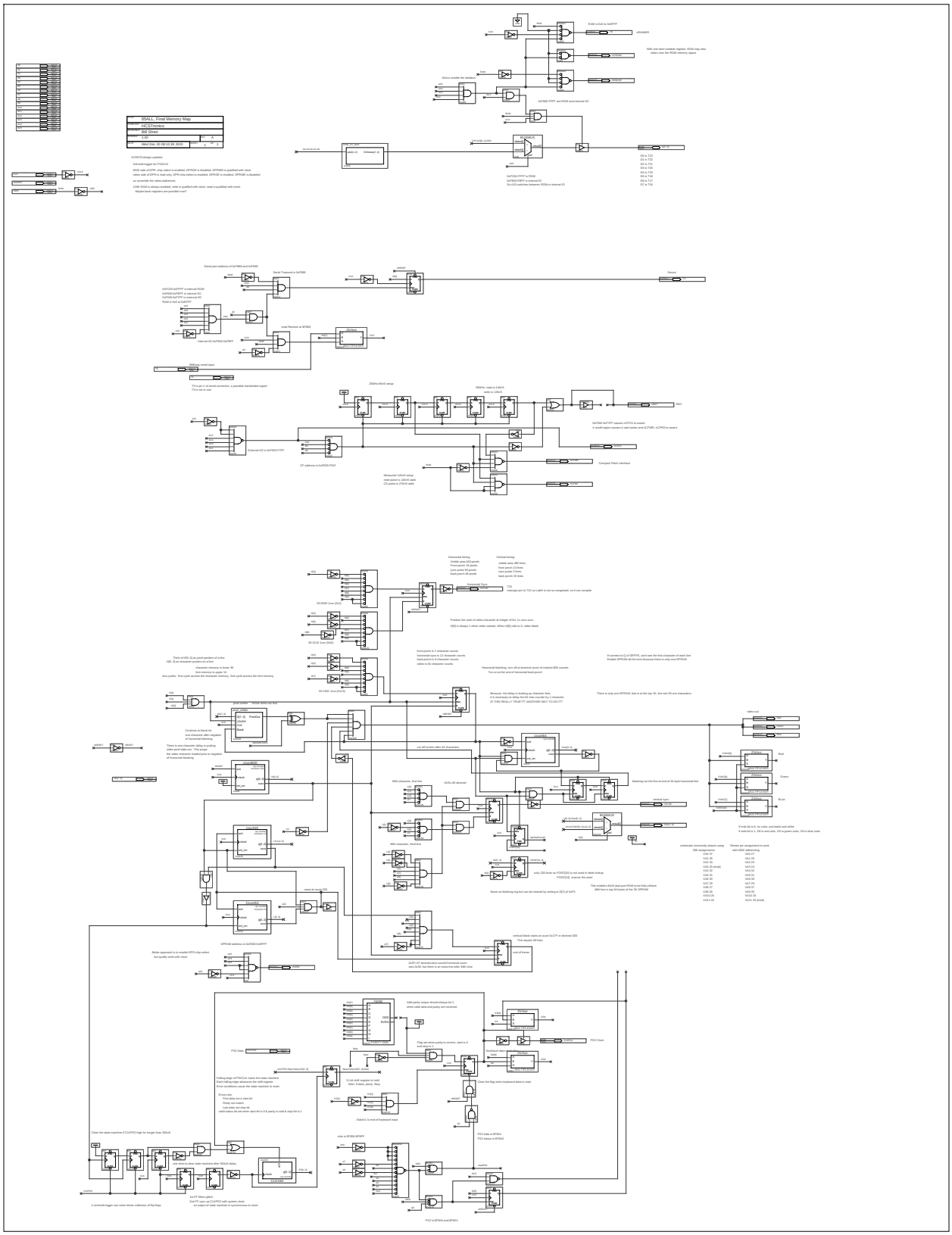
6SALL - Final Memory Map
BCSTronics
BB Shell
1.00
Wed Dec 20 00:33:28 2023
UCSX23 design options:
External trigger for PC2CLK
6502 side of DPR: chip select is enabled, DPRCE is disabled, DPRWR is qualified with clock
video side of DPR is read only, DPR chip select is enabled, DPRCE is enabled, DPRWR disabled
so scramble the video addresses.
1298: RAM is always enabled, write is qualified with clock, read is qualified with clock
Maybe bank registers are possible now?
0xFB00-FFFF are ROM and internal IO
0xFC00-FFFF is ROM
0xF800-FBFF is internal IO
Six 6116 switches between ROM or internal IO
Serial port address of 0xF800 and 0xF801
Serial Transmit to 0xF800
Serial Receiver at 0F800
Internal I/O 0xF800-0xF8FF
Compact Flash Interface
Horizontal timing
Vertical timing
Video RAM
Video ROM
Character ROM
Video Output
Sprite Data
Sprite Control
Sprite Position
Sprite Pointers
Sprite Multiplexer
Sprite Collision
Sprite Priority
Sprite Expansion
Sprite Enable
Sprite Color
Sprite Data Output
Sprite Data Shift
Sprite Data Latch
Sprite Data Mux
Sprite Data Output Mux
Sprite Data Output Latch
Sprite Data Output Shift