State_7FFC & SequentialRead need one more bit for the start command

One more ShiftData clock after RESETO

0xFFF: start, device address, read
0xFFE: address low (all zero)
0x1: sequential read, write to DRAM until
0x0: value in location 0, write to DRAM

DFFE

negate RESETO and let 68000 boot

That marks the end of serial loading

32763 is 0x7FFB

when not in the initialization states,

serDataRead

DummyWrite

shiftData

when 7FFE, low addr
7FFC, start
RF1: latch in the output of refresh timer, waiting for negation of AS
RF2: start of the refresh cycle
RF2.5: CAS asserts at the falling edge of clock
RF3: RAS asserts for 2 clocks

16us refresh with 8MHz clock input

make sure there are enough time for RAS precharge after the refresh is done
hold off clock until refresh finished
start the refresh when nAS is high

RF2.5: CAS asserts at the falling edge of clock
68000 timing is slower:
nAS is valid 335 after rising edge of S2, plenty of setup time for address valid at that time.
Assert RAS at falling edge of S2, then assert CAS at falling edge of S4

High if not CAS-before-RAS
Low during CAS-before-RAS cycle
High when CAS-before-RAS finished

0 wait states
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MemoryMap.bdf

- DRAM base is 0
- DUART base is FFF000
- IDE base is FFE000

Transcend CF works when IORD & IOWR are negate at same time as AS
But spec calls for early negation of IORD & IOWR (hold time), so add a clock of hold time

3 wait states for CF access
enable IORD & IOWR 2 wait state into access to give them 2 clock setup time

wait state generator

need more setup time for Transcend CF