1. **Video DTACK not connected**
   Connect U19 pin 1 to U37 pin 15

2. **DIP Component drill holes will only fit machine pin sockets**
   Need to increase drill size

3. **Ferrite bead footprint too small**
   Need to increase footprint in next version

4. **Memory footprint/pinout is incorrect for 628512 Static Ram**
   Use another socket between board and bend pins 3, 29, 31 of memory chip up. Connect pin 3 of memory chip to base pin 29, connect pin 29 of memory to base pin 31, and connect pin 31 of memory to base pin 3.

5. **VGA connector on board is incorrect**

6. **R55 and R6 silk screen identifiers are transposed on board for LED current limit**
   No impact to operation.

7. **Need to increase mounting hole size for PS/2 and ethernet connectors**
   Filing down the mounting pins you can make them fit.

8. **Diodes D6 - D10 are backwards on schematics and board**
   Schematic changes: reverse D6-D10 on the schematics.

   Be sure when you mount these diodes reverse to their silkscreen footprints or the diodes will become very hot

9. **Clocks for Bus Error (U35) and WAIT State generator (U12) are wrong**
   Schematic changes: U35 pin 9 is DS not AS*, U12 pin 9 is DS not AS*. Disconnect U25 pin 5 from GND. U25 pin 5 becomes DS* and pin 6 becomes DS. Connect a 4.7K to U25 pin 6 to VCC as a pull up.
   Connect U29 pin 20 to U25 pin 5. Connect U25 pin 6 to U35 pin 9. Cut traces labeled as #1 on PCB. (2 places on bottom and 1 on top).

10. **Chip Selects need to be qualified by AS* to be valid**
    Schematic changes: Add AS* to pin 13 of U36 and use new equations. Connect U33 pin 2 to U36 pin 13.

11. **Data Buffers are always on so memory reads are not valid**
    Schematic changes: Change pin 19 on U17,U10, and U31 from CPUSPC* to IOEN*. On U21 (byte decode) add CSROM to pin 6, CSRAM to pin 7, CSENET to pin 8 CSVRAM to pin 9, CSDRAM to pin 16, CSVIDR to pin17 and IOEN* to pin 19.

    Connect the corresponding pins from U36 to U17. Connect U17 pin 19 to U31 pin 19. Cut trace on top of board labeled 2 (note top trace between U31 and U36 near C46)

12. **Memory config wrong**
    Schematic changes: B0 on U23 pin 39 should be tied VCC not to ground.
    Cut trace labeled 3 on bottom of board near pin 39 on U23. Connect ping 39 to pin 42.

13. Mode Load for dynamic memory controller needs to be qualified by DRAM select.

Schematic Changes: U34 pin 3 from R/W* to MLCLK*. Add WR* to U24 pin 4 and MLCLK* to pin 17.

Cut trace labeled 4 on bottom of board near U34. Connect U24 pin 17 to U34 pin 3. Connect U21 pin 5 to U24 pin 4.