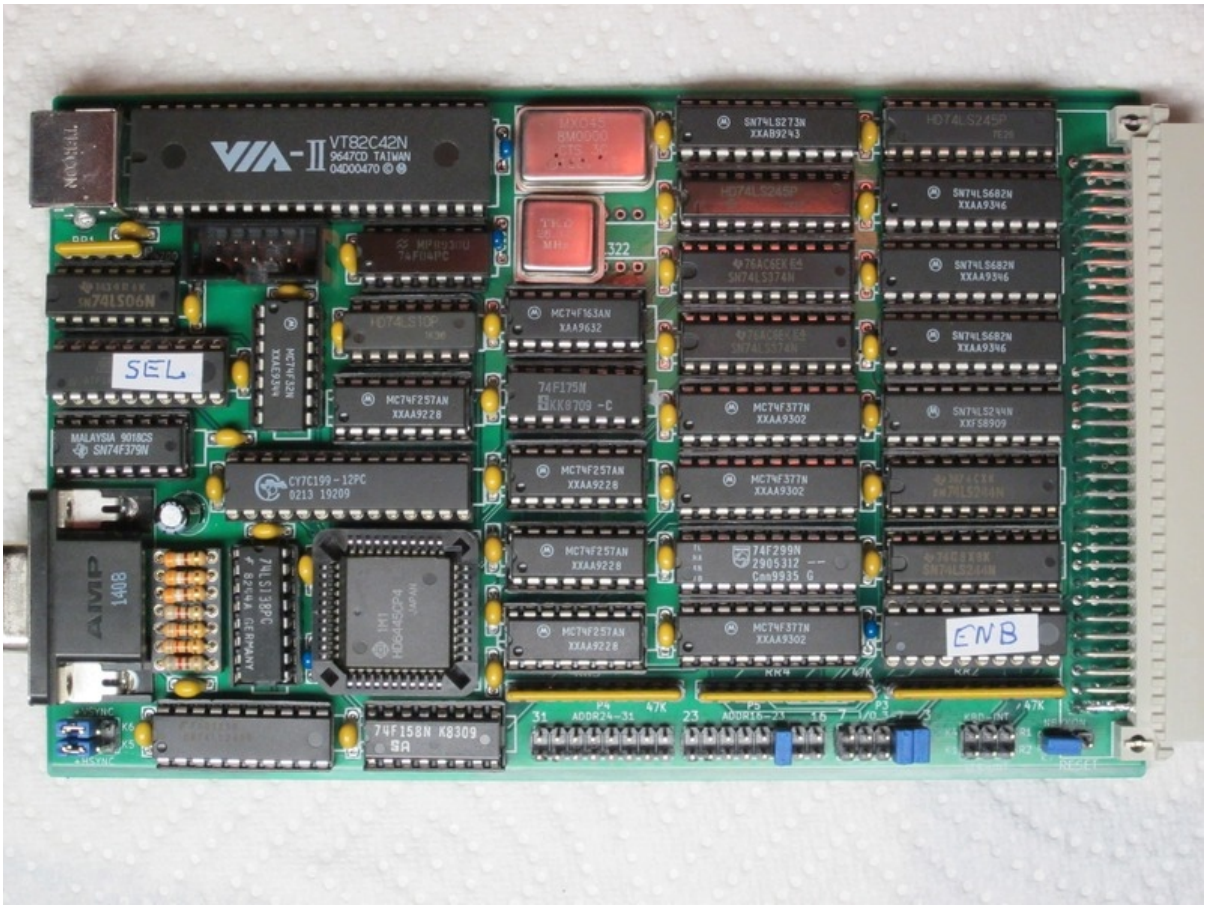
VGA3 – Programmers' Reference Manual – 1.1

Complete Board:



ECB bus Addressing:

P3 – selects the I/O address range A7..A3. Jumper off = '1'; jumper on = '0'. Above photo shows the board set for the address range $E0..$E7; viz., off, off, off, on, on.

P4,P5 – select the 64k memory mapped address range A31..A16. Unused address bits map to a 1 with pull-up resistors internal to the 74LS682 chips. Jumper off = '1' (or unused); jumper on = '0'. Above photo shows the board set for the SBC-188 address range $B000:0000 to $B000:FFFF, or $FFFBxxxx; viz., P4 all off, P5 off, off, off, off, off, on, off, off. VGA/MDA selection of the 32k actual address range is controlled by a bit in the CFG register on the board.

VGA3 board Addressing:

I/O+0
I/O+1: addresses the Keyboard Controller. (consult VIA VT82C42 data sheet for usage)

I/O+2
I/O+3: addresses the 6445 CRTC controller. (consult HD6445CP4 data sheet for usage)

I/O+4: VGA3 configuration register, CFG. (write only)

I/O+5: high order
I/O+6: low order; memory address register for CPU boards unable to support direct memory mapped addressing of the 32k memory chip. Both are (write only).

I/O+7: memory data byte addressed by the two bytes above. (read/write)

VGA3 configuration register (CFG):

The CFG register at I/O+4, $4E4 as shown above for the SBC-188, bits control various options on the board as follows:

Bit 7 (high order): B8/B0 bit. When set, the 32k memory is mapped to (P4,P5)+$8000 for memory-mapped access. When clear, 32k memory is mapped to (P4,P5)+0000.

Bits 6,5,4: Font2, font1, font0 address. These three bits define the 4k page containing the 8x16 font. Font0 is further modified by Font512, below.

Bit 3: Font512. Indicates that 2 fonts are in use, and bit 7 of the character attribute defines which font to use. The two fonts must be in adjacent 4K pages, starting at an even page.

Bit 2: Video Enable. Video is blanked when 0; enabled when 1.

Bit 1: reserved for future use. It was going to be “Oscillator Select.”

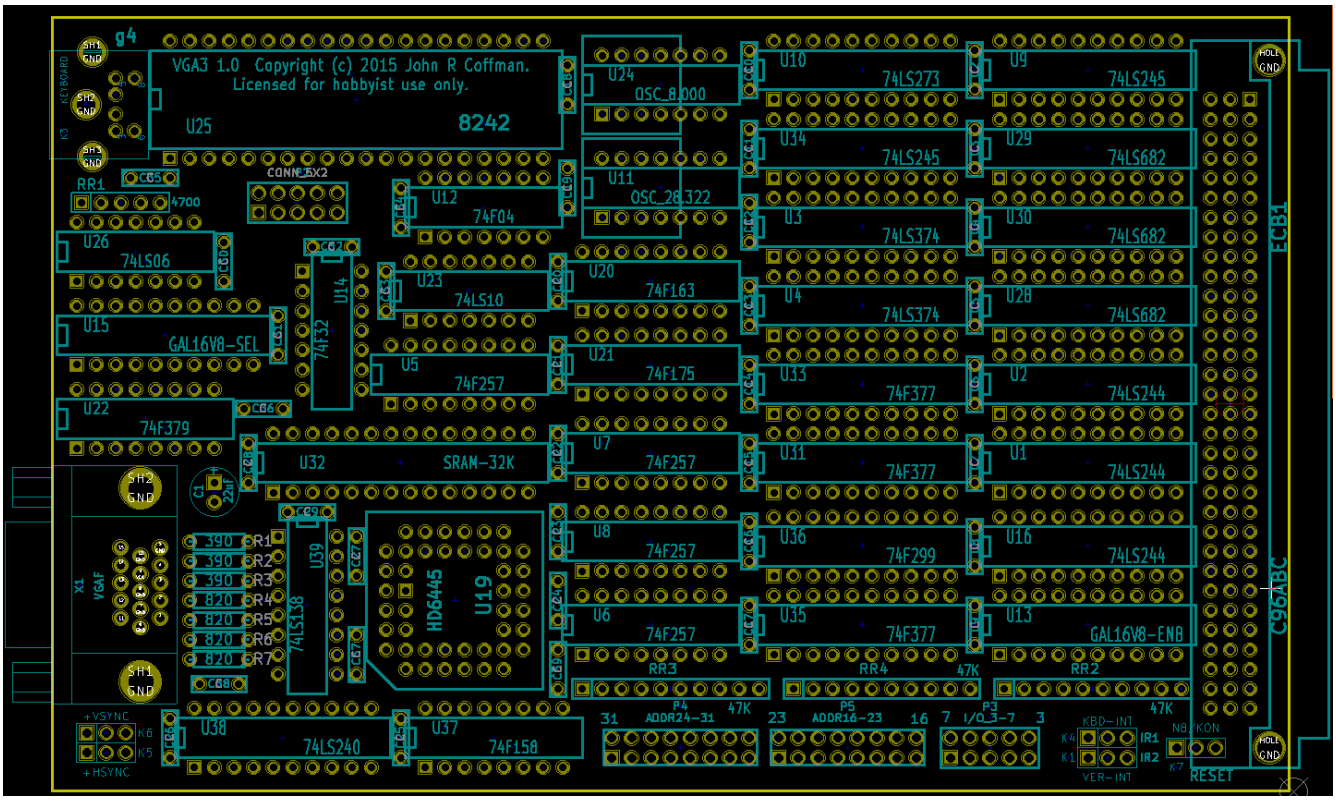
Bit 0: 8/9 character width. 8 pixel wide characters when ‘1’; 9 pixel wide characters when ‘0’.

The CFG register is cleared to zeroes on backplane “RESET.”

Status:

As of 06-May-2017, bit 7 of the CFG register is known to work; memory mapped data access is working; and address-register r/w access to memory is working.

Layout:



Chip Updates:

1. Update chips U1, U2, U3, U4 to 74ACT components
   U1, U2: 74LS244 → mc74act244 (74als good, too)
   U3, U4: 74LS374 → mc74act374
2. Add or replace C9, C11 with 10uF tantalum caps. Watch out for polarity. Solder to back of board if necessary. The fat tantalums won't fit between the IC sockets, so either install them last, or put them on the back of the board.
   C9 is next to pin 1 of U13, the ENB GAL.
   C11 is next to pin 1 of U34, the internal LS245.

The ACT chips apparently have longer turn-off delays than their LS counterparts, and the longer delay stabilizes memory addressing.

The 244 updates are not necessary for good operation on the SBC-188; I see no screen errors on the V3TPAT test; however, single digit memory errors are still reported by V3MTST. The change to ACT eliminates the V3MTST errors.

The 374 update is necessary for reliable operation on the Z180 Mark IV.

Jumpers:

Board I/O address P3 (for testing): 0xE0 = off, off, off, on, on

Address jumpers P4, P5 vary with CPU board. P4 address is always 0xFF = all off.

P5 address (A23..A16)
SBC-188 0x0B = off, off, off, off; off, on, off, off
Z180 Mark IV (not applicable)
Mini-M68k 0x37 = on, on, off, off; on, off, off, off (J4 on CPU board must be 'on'; J9 'off' for testing)
KISS-68030 0x0B = off, off, off, off; off, on, off, off (ROM w.s. 1 @ 25mhz, 2 @ 33mhz)

Sync jumpers for 80x25 mode: H: neg, V: pos. For 80x30 mode: H: neg, V: neg.

15-May-2017 jrc

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