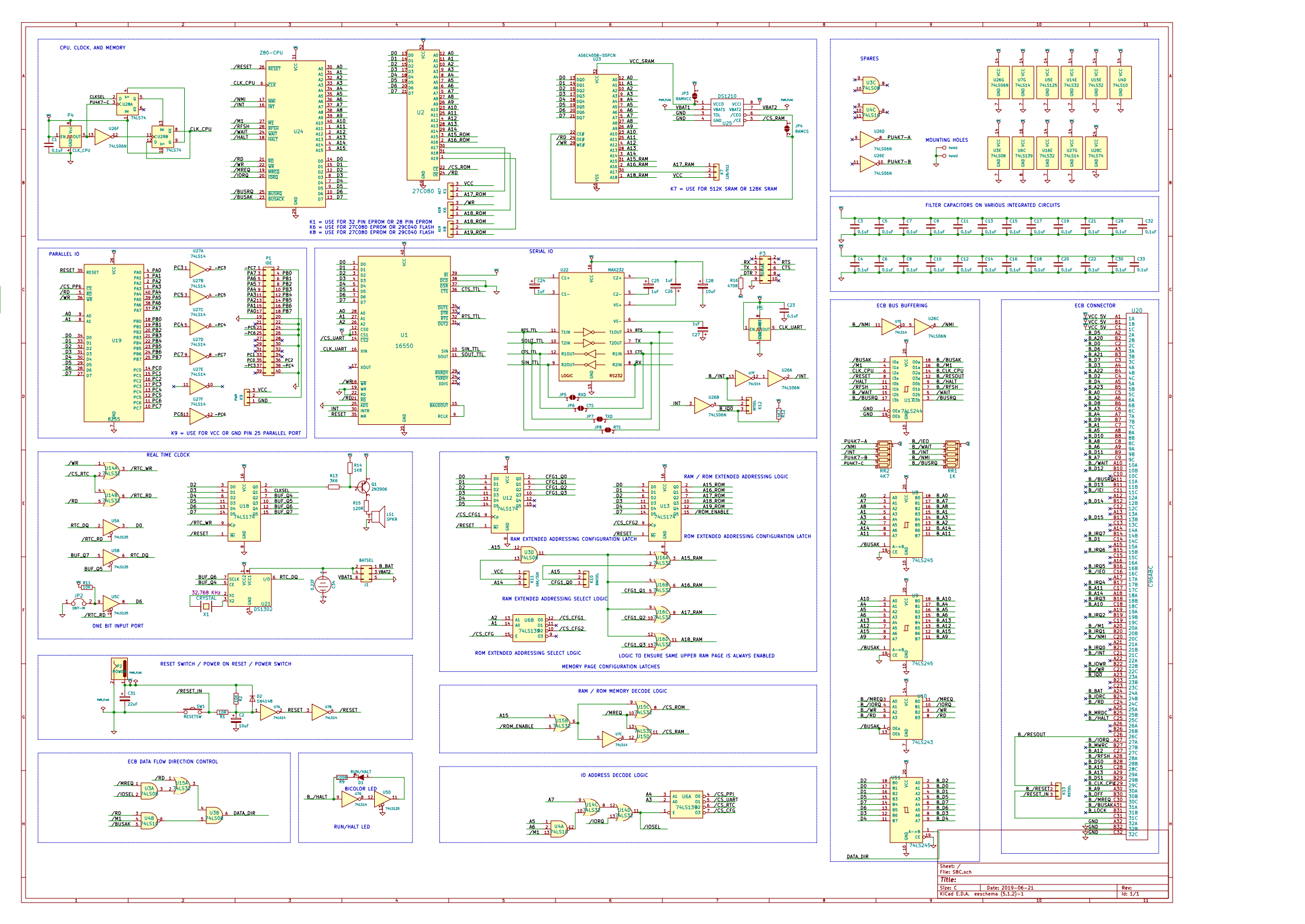
CPU, CLOCK, AND MEMORY
Z80-CPU
U24
U2
27C080
AS6C4008-55PCN
U23
VCC_SRAM
DS1210
U25
K1 = USE FOR 32 PIN EPROM OR 28 PIN EPROM
K6 = USE FOR 27C080 EPROM OR 29C040 FLASH
K8 = USE FOR 27C080 EPROM OR 29C040 FLASH
K7 = USE FOR 512K SRAM OR 128K SRAM
SPARES
MOUNTING HOLES
FILTER CAPACITORS ON VARIOUS INTEGRATED CIRCUITS
PARALLEL IO
U19
8255
K9 = USE FOR VCC OR GND PIN 25 PARALLEL PORT
SERIAL IO
U1
16550
U22
MAX232
ECB BUS BUFFERING
ECB CONNECTOR
REAL TIME CLOCK
U18
74LS174
DS1302
ONE BIT INPUT PORT
RAM / ROM EXTENDED ADDRESSING LOGIC
RAM EXTENDED ADDRESSING CONFIGURATION LATCH
ROM EXTENDED ADDRESSING CONFIGURATION LATCH
RAM EXTENDED ADDRESSING SELECT LOGIC
ROM EXTENDED ADDRESSING SELECT LOGIC
LOGIC TO ENSURE SAME UPPER RAM PAGE IS ALWAYS ENABLED
MEMORY PAGE CONFIGURATION LATCHES
RESET SWITCH / POWER ON RESET / POWER SWITCH
RAM / ROM MEMORY DECODE LOGIC
ECB DATA FLOW DIRECTION CONTROL
IO ADDRESS DECODE LOGIC
BICOLOR LED
RUN/HALT LED
Sheet: /
File: SBC.sch
Title:
Size: C
Date: 2019-06-21
Rev:
KiCad E.D.A. eeschema (5.1.2)-1
Id: 1/1