

Dual SDcard I/O Board
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The design of the Dual SDcard interface board was motivated by incomplete features on existing interfaces; namely, no access to the Card Detect information, which makes hot-swapping more coherent, and no access to the Write Protect switch setting on the card.

Write Protection is not a hardware feature of SD cards, but is a purely software operation. Hence, software must be aware of the setting of the write-protect switch on the card. Card hot-insertion and removal should also be detectable, and should be able to produce an interrupt, under program control.

The interface to the card should be based on the JUHA interface, beautiful for its simplicity and elegance.

To this end, a dual Secure Digital Card socketed board is proposed, with the following programming characteristics. Two cards are controlled by a single interface, which includes unit selection, card insertion/removal detection, and the ability to sense the state of the card Lock (write-protect) switch.

The board occupies two I/O addresses, one for an Operation Register, and the second a Selection Register. Both registers are read/write, although not all bits are writeable. The low order bit of the Selection Register selects the SD socket which is addressed by the Operation Register.

Format of the Operation Register:

bit 0: data bit I/O - reads as a data bit from the card, and writes as a data bit transmitted to the card

bit 1: clock bit - written to the card; the state of the clock bit may be read back

bit 2: chip select - must be set to one to assert the /CS line to the card. The state of the bit may be read back

bit 3: unused - reads back as zero

bit 4: write-protect - read-only state of the Lock switch on the selected unit; a '1' means the card is write-protected, '0' means it is writeable

bit 5: card detect - read-only card presence detect; '1' means a card is present in the socket of the selected unit, '0' means no card is present

bit 6: unused - reads back as zero

bit 7: unused - reads back as zero

When a card is not being accessed, Chip Select is kept at zero. The quiescent Clock state is also zero. During access to the card, Chip Select must be maintained at one, and the clock bit is toggled to clock data bits into or out of the card. Data is input to the card on the low to high transition of the clock, and data is output from the card to the host

computer likewise on the low to high transition of the clock. Byte data is transmitted and received MSB to LSB; i.e., bit 7 is first in or out, and bit 0 is last in or out.

The Selection Register controls Unit selection, Interrupt Enable, and Interrupt condition acknowledge. The register is read/write, and certain bits have different meanings on read than on write.

Format of the Selection Register:

bit 0: unit select – read/write, selects card slot 0, or card slot 1

bit 1: unused – reads back as zero

bit 2: read-only – Write Protect state of slot 0, will be '1' if card is locked or slot is empty

bit 3: read-only – Write Protect state of slot 1, will be '1' if card is locked or slot is empty

bit 4: reads as the state of the Card Detect switch for slot 0; will be '0' if the slot is empty, '1' if a card is present

writes as '1' or '0' to reflect the host's acknowledgment of the state of the Card Detect switch. When the software state and the hardware state of the switch disagree, an interrupt condition exists.

bit 5: same as bit 4, but for slot 1

bit 6: writes as the Interrupt Enable flag; '0' disables interrupts from either slot, '1' enables interrupts for card insertion/removal from either slot

reads as Interrupt Pending for slot 0, meaning the state of the hardware Card Detect switch differs from the software understanding of the state of the switch as written to bit 4.

bit 7: writes as the Change Enable for bits 4, 5, and 6. The state of these bits will not be changed on a write unless Change Enable is '1'.

reads as Interrupt Pending for slot 1, meaning the state of the hardware Card Detect switch differs from the software understanding of the state of the switch as written to bit 5.

Conventions on using the Selection Register include:

1. Simple unit selection. Because of the Change Enable bit unit selection consists of writing either "0x00" or "0x01" to the register.
2. Reading the register gives full information on the state of unit selection, and the state of Card Detect, Write Protect, and Card Insertion/Removal (Interrupt Pending) for both slots.
3. Clearing an interrupt consists of reading the Selection Register, OR-ing in a '1' to bit 7, and writing the register back out. This updates the software understanding of the state of the Card Detects to be the same as the hardware state of the switches.

At host computer hardware RESET, all bits in both the Operation Register and the Selection Register are cleared. This includes clearing the Interrupt Enable bit (bit 6) in the Selection Register, a bit which is not readable.

The 8-bit Z80 I/O address for the board is set with 7 board address jumpers. The Operation Register occupies the even address, and the Selection Register the odd address.

The board is compatible with the SBC v2, N8, SBC-188, Zeta, and mini-M68000.

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