
Subject: T80 (Z80) CPU in Multicomp

Posted by [nealcrook](#) on Sun, 11 Apr 2021 08:11:04 GMT

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TL;DR -> If you use T80 in an FPGA design, go get the latest version from <https://github.com/EisernSchild/t80>

Going back a few years, there was a lot of interest here in FPGA-based Z80 machines based on Grant Searle's "multicomp" design. The Z80 version used the synthesisable T80 core from opencores.org.

Recently I have been working on a reproduction of an old UK computer (the NASCOM 2) using that same core. When a "known good" CP/M boot loader failed to work I dived down a debug rabbit-hole which ended in the discovery that the T80 "ini" instruction did not work.

ini: read from port, store at (HL), increment HL, decrement B

On T80, HL does not increment. Finding this was "fun" especially as it was part of the floppy disk data load loop and so could not be single-stepped (with a WD2797 there is no data buffer and so data read/write is a real-time activity).

After a couple of hours looking at and simulating the T80 code, I did some internet searching and learned that this was a Known Bug (reported in the bugs list on [opencores](http://opencores.org)), and that T80 seems not be maintained on [opencores](http://opencores.org) any more. However, there is a maintained version/fork on github at <https://github.com/EisernSchild/t80>

I had to make one change to my code in order to switch from the [opencores](http://opencores.org) version to this version: the input clock port has been renamed from `clk_n` to `clk` (there is no change in function, this is just cosmetic).

So, if you are using this code, I suggest that you consider an upgrade.

Neal.
