Subject: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Fri, 08 Apr 2016 04:27:39 GMT
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All - I'm happy to announce the development of a new RBC SBC board, the SBC6120-RBC Edition

This is a re-layout of the Spare Time Gizmos SBC6120 into a 2-layer board routed in KiCAD.

I have setup a page for it on the Wiki here - SBC6120-RBC Edition

For those who aren't familiar with the SBC6120, it is a single board computer using the Harris HD-6120 "PDP-8 on a chip" which can be used to run vintage DEC software such as OS/8, FOCAL, and of course, Adventure! Robert Armstrong of Spare Time Gizmos licensed the design files under the GNU FDL and the software under the GPL, so I've taken advantage of that to create a new version of this workhorse board.

Right now I have a "minimum changes" version of the board already routed in FreeRouter. I've:
*Re-routed the board as a 2-layer board, with double-width traces for VCC and GND and flood-fills for VCC and GND on the top and bottom of the board.
*Added a jumper which allows either 27C256 EPROMS (original design) or 28C256 EEPROMs to be used (one of the address pins goes to a different location on the two chips).
*Made some slight changes to the POST display to allow standard rectangular LEDs to be used, and a slightly different reset switch.
*Tweaked a few locations of things to make the new silkscreens look better.
Everything else is unchanged from the original design.

Are there any other changes anyone would suggest before I go to prototypes on this?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Fri, 08 Apr 2016 20:57:52 GMT
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Sounds great Andrew.

Is your new board entirely compatible with the form factor of the original? I have one of Bob Armstrong's SBC6120's with a front panel, but I like some of the changes you are making (especially the EEPROM). I might be interested in swapping the host board and/or just having a working spare.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Fri, 08 Apr 2016 22:13:43 GMT

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The overall board footprint, mounting holes, and expansion/IDE/Serial connectors are all in the exact same locations. (I don't have the FP6120 front panel or the IOB6120 I/O expansion board, but I want to maintain compatibility with them)

The LEDs and reset switch shifted a little bit.

I'm also looking at switching the RAM from qty 3 64k x 4-bit HM6208s to qty 2 512k x 8-bit AS6C1008. The larger 32-pin 0.600" wide ICs will require moving a few of the other ICs on the board closer together, but if it I can get it to route in a reasonable way it will remove one of the "less standard" parts from the design which I think is a net improvement.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 10 Apr 2016 00:59:13 GMT
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Here's a new version with the 2 8-bit-wide SRAMs:

I think this is what I am going to go forward with for prototypes.

File Attachments
1) SBC6120-RBC-byteram.png, downloaded 2500 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sun, 10 Apr 2016 10:32:15 GMT
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Any suggestions for where one might source a Harris HD6120?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Sun, 10 Apr 2016 15:17:29 GMT
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UTSource

http://www.utsource.net/Product/Details/HD1-6120-8

That is where I got a couple previously.

Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by pbirkel on Sun, 10 Apr 2016 15:33:40 GMT
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Wayne W wrote on Sun, 10 April 2016 08:17UTSource

http://www.utsource.net/Product/Details/HD1-6120-8

That is where I got a couple previously.

Wayne

Try: http://www.utsource.net/ic-datasheet/HD1-6120-8-701534.html

Although the part-description is a bit ... discouraging :-<.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Sun, 10 Apr 2016 17:11:51 GMT
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As I've emailed Andrew privately, this is tremendous - Bob Armstrong's design is fantastic, but hasn't been available for some time.

Kudo's to Andrew for reproducing the PC board!

I wouldn't worry about the SRAM personally - the 64Kx4 types have many equivalents. I used Sharp LH52252AD-45's in the boards I built in the past. We could certainly arrange a bulk purchase of CPU/SRAM/GAL's for folks.

The HD1-6120's come in -2, -8 and -9 varieties. All work fine (the only difference is that the -9 is commercial temperature rated, the other two have a slightly wider range.

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 10 Apr 2016 17:26:40 GMT
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The RAM change is something that a lot of people have asked Bob for over the years, since I've got it all routed I'm going to go ahead with it for my initial run of prototypes. If it poses any kind of a problem, we'll go back to the original design.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sun, 10 Apr 2016 18:34:18 GMT
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Brilliant, ordered the CPU, please put me down for a prototype board.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 10 Apr 2016 20:55:57 GMT
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I'm planning to do a run of 5 prototypes, so far I have Gary and Will and myself down for 3 of them.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Mon, 11 Apr 2016 01:14:10 GMT
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pbirkel wrote on Sun, 10 April 2016 08:33Wayne W wrote on Sun, 10 April 2016 08:17UTSource

http://www.utsource.net/Product/Details/HD1-6120-8

That is where I got a couple previously.

Wayne

Try: http://www.utsource.net/ic-datasheet/HD1-6120-8-701534.html

Although the part-description is a bit ... discouraging :-<.

Yeah, I assume the description is just wrong. Not totally unusual for UTSource to have the wrong description or picture. I have never had a problem getting the correct part though. I got two of this exact part from them in January 2015.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 11 Apr 2016 05:04:53 GMT
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The 5 prototype boards are spoken for at this point:
Me
Gary (has original STG board as well)
Wayne (has original STG board as well)

John C.
1 gentleman from the Spare Time Gizmos group who contributed a fixed Gerber of the original board to help get this done.

Should be about 2 weeks to get them in.

I am really glad to get this board re-captured into an open source EDA program and available for other hobbyists. It's a very well thought out design and the BTS6120 monitor ROM is very powerful!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Mon, 11 Apr 2016 15:03:06 GMT
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Fantastic!

I should have all parts waiting here for construction. (Just saw new diagrams on the Wiki, using 128Kx8's)

As a follow up project, might be neat to have a S-100 "carrier" board with a simplified front panel that the SBC6120-RBC can piggy-back onto

- Gary

Andrew B wrote on Sun, 10 April 2016 22:04The 5 prototype boards are spoken for at this point:
Me
Gary (has original STG board as well)
Wayne (has original STG board as well)
John C.
1 gentleman from the Spare Time Gizmos group who contributed a fixed Gerber of the original board to help get this done.

Should be about 2 weeks to get them in.

I am really glad to get this board re-captured into an open source EDA program and available for other hobbyists. It's a very well thought out design and the BTS6120 monitor ROM is very powerful!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 11 Apr 2016 19:59:07 GMT
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Changes from the original board in the BOM:

*RAM is 2x AS6C1008-55 (either -55PCN or -55PIN should work).

*POST LEDs are 4x rectangular 5mm x 2mm w/2.54mm lead spacing - Digikey example Jameco example

*Each post LED needs a 150 ohm resistor (yields a 20ma LED current)

*Reset switch is a switch with the spacing between the pins at 4.5 mm, the spacing between the mechanical "legs" at 7.0 mm, spacing between the two sets of holes at 2.5 mm, and a plunger depth of ~5.85-6.00 mm - Digikey example Jameco example (there are several switches which will fit made by different manufacturers).

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Tue, 12 Apr 2016 18:54:32 GMT
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Andrew B wrote on Sun, 10 April 2016 22:04The 5 prototype boards are spoken for at this point:
Me
Gary (has original STG board as well)
Wayne (has original STG board as well)
John C.
1 gentleman from the Spare Time Gizmos group who contributed a fixed Gerber of the original board to help get this done.

Should be about 2 weeks to get them in.

I am really glad to get this board re-captured into an open source EDA program and available for other hobbyists. It's a very well thought out design and the BTS6120 monitor ROM is very powerful!

Sounds great Andrew. I have a couple of spare HD6120 already, so I am good on the hardest to procure part. I will review the rest of the parts list shortly and try to get everything ahead of the board's arrival.

As I reviewed the state of my previous build, the one point of frustration for me was the ROM versions. Based on email's from Bob Armstrong, the latest ROM version is 271 (ignoring a branch of ROM version for the -RC hardware version which is not relevant). However, the only ROM version source/hex files I have ever found are 266. I asked for the latest version on the SpareTimeGizmos Yahoo! Forum some time ago, but radio silence. If you have any contacts that might be able to get us the latest version, that would be very nice. Not a show-stopper since v266 should be quite functional.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition

Posted by gkaufman on Tue, 12 Apr 2016 19:02:29 GMT
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Wayne -

I'm fairly certain I have the 271 version of the ROM at home. I'll check tonight and can upload it to the wiki.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 12 Apr 2016 19:04:19 GMT
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My plan is to get a working board and then ask about the source code for v271. Another person (Jim Kearney who designed the IOB6120) contributed code to the monitor ROM at one point and his code is licensed under the GPL, so the source code for the later versions should be made available to anyone who received a binary versions in the ROM.....

v271 fixed some bugs in the fron panel switches/rotary knob, so it would be nice to have that version. Otherwise we'll need to start from v266 and re-create the fixes.

But I think once we have working boards, it's very likely I'll be able to get us a copy of the source.

I'd be hesitant to upload the binary version to the wiki without the source due to the GPLed code.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Tue, 12 Apr 2016 20:10:55 GMT
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gkaufman wrote on Tue, 12 April 2016 12:02Wayne -

I'm fairly certain I have the 271 version of the ROM at home. I'll check tonight and can upload it to the wiki.

That would be great. I would love to upgrade my current board at this point.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Tue, 12 Apr 2016 21:41:08 GMT
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Wayne -

I uploaded what I think is a later version of the design files to the Wiki at:
https:// www.retrobrewcomputers.org/doku.php?id=boards:sbc:sbc6120-rb c-edition:start

Unfortunately I don't see any source for the v2.71 ROM's, but the .hex files are there.

I'll keep looking thru my somewhat disorganized downloads to see if I have more.

- Gary

Wayne W wrote on Tue, 12 April 2016 13:10gkaufman wrote on Tue, 12 April 2016 12:02Wayne -

I'm fairly certain I have the 271 version of the ROM at home. I'll check tonight and can upload it to the wiki.

That would be great. I would love to upgrade my current board at this point.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Tue, 12 Apr 2016 22:25:50 GMT
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Hope it was ok to upload the files to the WIKI, but it's a file that I believe came from Bob's site in the past and includes all of the original license info.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 12 Apr 2016 22:38:52 GMT
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Regardless of what was up on Bob's site, if we have a v271 binary on the wiki, we technically need to have the v271 source available as well - since Jim K's code contributions are under the GPL which requires the source be offered with the binary.

I'll take it down later (only admins can delete things right now...)

My plan was to link to the resources on the STG site on the wiki for now until we have working boards at which point I'll make new RBC Edition Design and Source archives for the wiki with all the appropriate license info.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Tue, 12 Apr 2016 23:13:02 GMT
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Andrew B wrote on Tue, 12 April 2016 15:38Regardless of what was up on Bob's site, if we have a v271 binary on the wiki, we technically need to have the v271 source available as well - since Jim K's code contributions are under the GPL which requires the source be offered with the binary.

I'll take it down later (only admins can delete things right now...)

My plan was to link to the resources on the STG site on the wiki for now until we have working boards at which point I'll make new RBC Edition Design and Source archives for the wiki with all the appropriate license info.

OK, understood. Hopefully, the v271 sources are available. They are definitely not posted on the STG site.

Appreciate your efforts Gary.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 13 Apr 2016 01:07:09 GMT
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Found the Source for 2.71!

Appended.

Andrew, hopefully we can re-zip this in with the file I previously posted and satisfy the GPL?

- Gary

File Attachments
1) BTS6120.PLX, downloaded 559 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Wed, 13 Apr 2016 01:38:54 GMT
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gkaufman wrote on Tue, 12 April 2016 18:07Found the Source for 2.71!

Appended.

Andrew, hopefully we can re-zip this in with the file I previously posted and satisfy the GPL?

- Gary

Excellent. Thanks Gary!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 13 Apr 2016 01:51:54 GMT
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AWESOME! You made my day!

Yeah, as long as they are in the same .zip it will be fine.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 13 Apr 2016 03:04:17 GMT
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Ok, updated the .zip file on the WIKI to include the source.

Sometimes being a pack rat pays off

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by computerdoc on Wed, 13 Apr 2016 08:05:31 GMT
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Hi Gary,
I agree Gary! I wish I could convince my family that being a pack rat is a good thing.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 19 Apr 2016 17:05:38 GMT
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I received the shipping notice that the prototype boards are on their way to me via DHL Express from Hong Kong. Since I am on the "left coast" (15 minutes from LAX) I expect they will be in my hands by the end of the week.

I spent the weekend searching over 50 independent stocking distributor websites in the US hoping to find some HD1-6120-2,8,9s for this project from a source other than China. A handful (~5) supposedly had stock. So far only one distributor has replied to my RFQs saying they had any of them available, and they wanted $75 each

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by jcoffman on Tue, 19 Apr 2016 17:50:00 GMT
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I have found both the 6120 & 6402 on eBay for $16 & $5, respectively. Both, of course, are coming from China.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 19 Apr 2016 18:03:06 GMT
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Jameco has the 6402, they are pulls but I'd trust them over China - http://www.jameco.com/webapp/wcs/stores/servlet/Product_1000 1_10001_43158_-1

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Tue, 19 Apr 2016 18:24:53 GMT
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u-barn? they shipped me 2 bogus Z80 SIO chips. After I complained I got the right ones.
Make sure you check the wares

RHK

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Tue, 19 Apr 2016 18:26:14 GMT
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I also believe that many 5v only standard UART will interchange. Fortunately I have a few 6402's in the parts draw.

I've purchased 6120's from China in the past, and just received one from UTSource last night. I'll test it shortly and report back to the group, but it looks like a clean new part.

Excited to get the board, all parts are now here...

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 19 Apr 2016 22:37:37 GMT
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Delivery date is confirmed as Thursday (6/21).

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 20 Apr 2016 10:49:49 GMT
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Tested the Intersil HD1-6120-8 from UTSource last nite, worked fine in a SBC-6120 using 5mhz clock (higher speed not tested).
Purchased thru their phone app, so after 10% discount price was $18.75 + $2.00 shipping. 14 days to arrive.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 20 Apr 2016 15:34:11 GMT
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Could you post some pictures of the chip? I'm curious, I feel like they may be remarked (Harris only became Intersil in 1999, which I believe was after the 6120 was discontinued) but I can't think of why that was needed.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 20 Apr 2016 18:23:06 GMT
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Looks like the part in auction #311454981484

Light colored ceramic, etched markings, clean pins.

Andrew B wrote on Wed, 20 April 2016 08:34Could you post some pictures of the chip? I'm curious, I feel like they may be remarked (Harris only became Intersil in 1999, which I believe was after the 6120 was discontinued) but I can't think of why that was needed.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Fri, 22 Apr 2016 03:45:27 GMT
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The boards are here!

File Attachments
1) SBC6120-RBC (Small).jpg, downloaded 2379 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Fri, 22 Apr 2016 13:54:55 GMT
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Very nice!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 23 Apr 2016 22:12:10 GMT
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Prototype boards shipped out to Gary, Wayne, John & Will today.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 24 Apr 2016 16:13:53 GMT
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I built up my prototype board yesterday.

No magic smoke! But no POST either Dug out my Open Bench Logic Sniffer....

The HD-6120 has power, ground, clock, I can see it indicating /RUN is high during /RESET when I push the reset button and then coming back online, and the CPU sending out instruction fetch cycles...

THe BTS6120 POST routine is pretty extensive, if the ROMs and the POST code display are working it will change the POST LEDs even before testing the RAM.

A few possibilities at this point:
-I made some kind of screwup on the board layout.
-My 22V10s are not programmed properly. I did some file hacking to allow my Chinese programmer to actually program the 22V10s. The software said it was able to both program and read back the fuse maps, but it's still suspect.

I'll keep everyone posted..heh... if you want to build your boards and help with debugging that's great, or if you want to wait I totally understand, a cut & jumper fix if required will be way easier on an unbuilt board.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Mon, 25 Apr 2016 01:58:04 GMT
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Andrew -

You should receive the 22V10's and 16V8 I programmed for you in tomorrow's mail. Finger's

crossed.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 25 Apr 2016 05:11:56 GMT
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Yeah, I've done a lot of chip swapping today figuring things out. I managed to get the chips out of my original board (machine tooled sockets + not perfectly formed DIP leads with some outward preload on them = super super hard to remove....and the decoupling caps being so close to the sockets in the original board design don't help either) and piggyback in some dual swipe slots to make swapping things in and out easier for testing.

Confirmed that my MEM GAL and ROMs are good and work in a the STG board (I made 28C256->27C256 pinout adapters out of some some sockets by cutting off pin 1 on the bottom of the socket, adding a small jumper line between Pin 27 -> Pin 1 under the IC, and bending out Pin 27 of the IC to make the 28C256s work in the original Spare Time Gizmos boards). IOT GALs are no good.

However, even with all of the known working chips out of the original STG board, the new board doesn't work.

I also reviewed the schematic for the SBC boards, and found a pretty huge mistake.

The memory address order on the ROM chips follows a strange order, and I totally missed reproducing that when I laid out the board and screwed it up.

Here's the relevant part of the original SBC6120 schematic:

And he's my schematic:

(Note that because KiCAD doesn't support "heterogeneous buses" with different designations within the bus like MA, EMA, etc, I changed the extended memory address signals EMA0, EMA1, and EMA2 to MA12, MA13, and MA14 for the purposes of routing the buses cleanly around the different parts of the schematic. I went back and confirmed that at least I did that right..... .

In order for these boards to work one of two things has to happen:
-An adapter shim needs to be made to plug into the sockets, or the ROMs need to be put off to the side on a breadboard, such that the address lines are switched back to their correct order.
-We need to write a Python script to load the Intel hex file, make a pair out of each address/8-bit byte of data, exchange the address bits as they are switched in the hardware, sort the pairs by address, and output a modified hex file such that each address outputs the correct byte of data even though the lines are scrambled.

So sorry guys, I feel like an idiot. I can probably design up a simple adapter board that will make the fix a little more cleanly for the 4 of you and have some made....

File Attachments
1) SBC6120-ROMs.png, downloaded 1302 times
2) SBC6120-RBC-ROMS.png, downloaded 1441 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Garth on Mon, 25 Apr 2016 05:47:21 GMT
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If you make an adapter to de-scramble the lines, just make a single one for programming, instead of one for each board produced. (See if it's easier than writing your Python script to de-scramble it.)

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 25 Apr 2016 06:11:00 GMT
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The nice thing about the Python script is that Will is in the UK and it saves on postage ;)

There is already a library for Intel Hex files (https://pypi.python.org/pypi/IntelHex/1.5 so it looks like it should not be hard to do this in software. Create 2 IntelHex objects. Load the original file into one. Step through each address starting with 0. Write the byte at that address to the corresponding 'scrambled' address. Write out the new file at the end.

(I'm also working on a breadboard de-scrambler just as a sanity check)

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 25 Apr 2016 09:38:25 GMT
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Hi guys

I think a little Python script is in order. It's just a matter of putting the data in the "right" place in ROM in order to match the scrambled address lines. Funnily enough I was idly daydreaming in the shower about pretty much this yesterday -- I was thinking the order of the address pins to a RAM really don't matter, but if you scramble the address pins to a ROM you have to scramble the contents to match.

Anyway, easily fixed with a little software. And as you say the postage for software is $0

My suggestion: Use srecord to convert to binary, use a python script to appropriately scramble the binaries, then use srecord to convert back to the format your programmer expects (or just feed the binary direct to your programmer, which is what I plan to do).

PS I am very happy to write this script. Can you provide the ROM hex input file? I'll have a bash

this evening.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Mon, 25 Apr 2016 12:51:55 GMT
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Will -

Look here in the SW sub-directory (271L.HEX and 271H.HEX)

https://www.retrobrewcomputers.org/lib/exe/fetch.php?media=boards:sbc:sbc6120-rbc-edition:sbc6120_design.zip

will wrote on Mon, 25 April 2016 02:38Hi guys
PS I am very happy to write this script. Can you provide the ROM hex input file? I'll have a bash this evening.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 25 Apr 2016 14:13:34 GMT
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Try the attached.

Contents as per the "SW" directory, with these additions:

romscrambler: A short python script to scramble the ROM contents

scramble: A shell script which uses srecord to convert the high/low HEX files to binary, scrambles them, then converts the resulting binaries back to intel HEX format.

The other files are the output of running the "scramble" script:

271L.ROM, 271H.ROM: Binary versions of 271L.HEX, 271H.HEX

271L-SCR.ROM, 271H-SCR.ROM: Scrambled ROMs (binary version)

271L-SCR.HEX, 271H-SCR.HEX: Scrambled ROMs (intel hex version)

Let me know if it works!

Will

Copy of the "romscrambler" script follows for those who don't want to download the .tar.gz just to

see it:

```
#!/usr/bin/env python

import sys

# map of address pin connections: bus address line -> ROM address line
addr_line_map = {
        0: 11,
        1: 10,
        2: 9,
        3: 8,
        4: 7,
        5: 6,
        6: 5,
        7: 4,
        8: 3,
        9: 2,
        10: 1,
        11: 0,
        12: 14,
        13: 13, # we got one right!
        14: 12,
        }

def scramble_addr(busaddr):
    romaddr = 0
    for bus_bit, rom_bit in addr_line_map.iteritems():
        if busaddr & (1 << bus_bit):
            romaddr |= (1 << rom_bit)
    return romaddr

if __name__ == '__main__':
    # check command line arguments
    if len(sys.argv) != 3:
        print "syntax: %s [inputfile] [outputfile]" % sys.argv[0]
        sys.exit(1)

    # start with an empty ROM (0xFF = unprogrammed byte)
    data_out = [chr(0xFF)] * (2**len(addr_line_map))

    # load data from input file
    data_in = open(sys.argv[1], 'rb').read()
    if len(data_in) > len(data_out):
        print "Error: input file larger than expected (max %d bytes)" % len(data_out)
        sys.exit(1)
```

```
# scramble it
for addr, value in enumerate(data_in):
    data_out[scramble_addr(addr)] = value

# write result to output file
open(sys.argv[2], 'wb').write(''.join(data_out))
```

File Attachments

1) SW-scrambled.tar.gz, downloaded 463 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 25 Apr 2016 19:48:05 GMT
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will - thanks for the sweet code! I will try the 'scrambled' ROMs as soon as I get home tonight.

Indeed, the RAM address lines also had a strange order on the original SBC6120. I asked Robert Armstrong about that and it turns out the original board was a hand-layout, the order made the layout a bit easier. Since I was using Freerouting (and different RAM chips) I switched the order back to match the chip pins.

I totally missed the ROM order in the process though.

Assuming the modified ROMs work - do you guys think I should do another board rev to fix the order to maintain chip to chip ROM compatibility with the original boards - or we could standardize on re-ordered ROMs for the RBC version so the address lines match up.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 25 Apr 2016 20:05:41 GMT
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I'd re-spin the board for the final run to maximise compatibility with the original SBC6120.

There will be just five machines in the world that need the special ROM scrambling

It think ROM updates are likely to be infrequent so this is unlikely to be a headache even for those five builders.

Just doing my parts order now -- which switch did you have in mind to fit the new S1 footprint?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 25 Apr 2016 22:07:03 GMT

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will wrote on Mon, 25 April 2016 13:05
Just doing my parts order now -- which switch did you have in mind to fit the new S1 footprint?

https://www.retrobrewcomputers.org/forum/index.php?t=msg&amp ;th=51&goto=471&#msg_471

I bought the Digikey example part listed in my prior post.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 25 Apr 2016 22:20:15 GMT
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Ah, rats. I should have read more carefully. Never mind, just went digging through my parts bin looking for a chip and came across exactly that type of switch, I think it is a spare left over from building the Zeta 2 -- so I've got something suitable.

I went with the original quad LED part too so I will fit wire jumpers at R11--R14.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 25 Apr 2016 22:45:12 GMT
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You might want to fit check that, I realized after I made the boards that the resistors may need to be .010" farther back from the LED footprints for the original LEDs to fit (or you might need to put the jumper wires on the bottom of the board and cut the joints flush on the top of the board for it to fit.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 25 Apr 2016 23:10:01 GMT
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Thanks for the tip -- normally I would have fitted the LEDs last. I shall report back on what seems possible.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 25 Apr 2016 23:12:47 GMT
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PS reading about the PDP-8 it seems they number their bits backwards! (I suppose there was little precedent to copy)

So I may have got the mapping reversed in the program -- but it's easy and hopefully obvious how to reverse it.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Tue, 26 Apr 2016 11:01:23 GMT
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Hi Andrew

Can you please advise - does the IDE interface supply power on pin 20 so that it can be used to power an IDE to CF adapter? The STG user manual indicates pin 20 on the IDE is no-connect, so could one just easily patch in a connection to VCC?

Thanks

Will

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 26 Apr 2016 15:05:56 GMT
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IDE Pin 20 is NC just like the original board.

I could probably add a jumper to feed VCC to that pin in the final revision.

Just a running list of updates so far:
1. Fix ROM address line order
2. Move LEDs resistors slightly away from LEDs
3. Add jumper to feed VCC to IDE pin 20

Since the address line order was already take into account on the original schematic, your Python code should work fine. I got caught up with some other stuff last night and it will probably be tonight before I can try it.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Tue, 26 Apr 2016 16:35:19 GMT
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Yes a jumper to VCC would be a good idea. Even better would be a footprint with 0.2" spacing to take a PPTC -- I now fit these in place of a jumper on all my IDE boards. If you accidentally plug a CF adapter in one pin out of alignment it can short VCC to GND, I burned out a trace on my Mark IV SBC this way! The PPTC would trip before any traces burn out. It is possible to fit them to 0.1" spaced holes but it's a bit untidy; 0.2" would be perfect.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Tue, 26 Apr 2016 18:16:34 GMT
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Board arrived yesterday, unfortunately I arrived home too late to start construction.

At this point I'll probably wait to hear if the scrambled roms work properly, but the board looks very nice!

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 27 Apr 2016 05:33:01 GMT
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Well, with the 're-arranged' .HEX files from Will, and a set of GALs from Gary (verified to work in my original STG board) I get POST codes up to 'Memory test error' per Page 18 of the SBC6120 User's Guide.

However: I was pressing on/seating some of the chips on my board, and the post codes went all the way to the 'BTS6120 running' and a string of register values from the ROM monitor displayed on the serial terminal. So it seems likely that I *may* be having some problem with this specific board, and not the design.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 27 Apr 2016 15:51:20 GMT
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Anyone got a suggestion for how I can program these Atmel ATF22V10C GALs?

I have an Autoelectric TL866A programmer.

I have programmed the ATF16V8B but my programmer does not seem to support the ATF22V10C.

As an alternative I have several Lattice GAL22V10C chips left over from the KISS-68030 build. I believe these would be an acceptable substitute but I am not 100% sure -- can anyone throw light on this?

Thanks!

Will

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by ab0tj on Wed, 27 Apr 2016 15:53:48 GMT
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Hi Will,

I did not have success programming either brand of 22V10 chip with my TL866A. It sounds like others have been able to make the Lattice chips work, but not the Atmel chips. I ended up ordering a Wellon programmer which seems to program both brands with ease.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 27 Apr 2016 16:35:19 GMT
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Hey

I have got the GAL22V10C chips programmed with the IOT1 and IOT2 code. I really just want to confirm that they are drop-in replacements for the ATF22V10C in this circuit -- ie avoid blowing anything up!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 27 Apr 2016 17:41:06 GMT
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I have used both Atmel and Lattice 22V10's in the SBC6120 without difficulty.

I have also never had luck programming 22V10's on the TL866A.

I'm happy to program the GAL's for folks as long as they send them to me and provide a return mailer or cover shipping.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 27 Apr 2016 17:46:50 GMT
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Gary

ATF22V10C and GAL22V10C both programmed and verified fine with the TL866A for me. I assume this means they will work.

Thank you for the confirmation that GAL22V10C can be used in the SBC6120 circuit. That's what I will try.

I did have one GAL22V10C which did not work in the KISS-68030; I replaced it with another chip

programmed identically and it worked fine. The GAL22V10Cs I have are all second-hand chips that have been pulled from other systems so I concluded that the chip had suffered some sort of "incident" before it came to me.

Will

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 27 Apr 2016 19:47:32 GMT
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The Lattice GAL16V8 and GAL22V10 parts Gary programmed for me work fine in my original STG board. So it looks like the .JED files can be used to program either GAL or ATF parts, and either part will work in the boards.

However, one thing to note is that the programming algorithm is different for the ATF and GAL parts, so you want to make sure that your programmer is setup for the correct parts.

When I get home tonight I plan to do some more probing with my logic analyzer and see if I can figure out what's up with the RAM test on my board. It writes 0's and -1s to the RAM and reads them back, should be pretty easy to see what's up.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 28 Apr 2016 16:00:25 GMT
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Just an update:

With my logic analyzer I've been able to see the board working its way through the ROM bootstrap code. It sets POST code 7, then tests the CPU, then sets POST code 6, does a really simple test of a couple words of RAM to make sure reading and writing works, copies a ROM bootstrap into RAM, then starts copying the contents of the ROM over to RAM.

I've still trying to trace out POST 5 and POST 4 (which is where it's hanging up). It seems like it's getting stuck in an infinite loop of JMPs for some reason. I only have 16 channels of my logic analyzer so I'm basically watching the data bus, /RESET, /READ, /WRITE, and /RAM_CS.

Since so many things are working so well, this is kind of maddening!

Hopefully tonight I'll be able to check what's going on around the other two post codes and figure out where this infinite loop is coming from.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Fri, 29 Apr 2016 04:30:05 GMT

It's alive!!!

(If you don't want to read all this, skip to the bottom for the 1 jumper wire that needs to be soldered on as a fix).

I traced out the POST process with my Open Bench Logic Sniffer, specifically honing in on POST code #4 where the board is hanging. The relevant section of code from the ROM monitor is:

```
; Make sure that panel memory and main memory are distinct...
 POST+4   ; set the POST code to four
 STA   ; put -1 in location 0 of panel memory
 DCA @[0]  ; ...
 CPD   ; and then put 0 in the same location
 DCA @[0]  ;  ... of main memory
 SPD   ; back to panel memory
 ISZ @[0]  ; and increment -1
  JMP    .  ; if it doesn't skip something is wrong
```

I looked at DX11-DX0, the POST11 LED signal, /READ, /WRITE, and /RAM_CS:

Above we can see the POST code being set to 4 (first cursor), -1 being written to location 0 of main memory (second cursor) and 0 being written to location 0 of panel memory (third cursor). However, when the CPU reads back location 0 of what is supposed to be main memory (=-1) it gets 0, increments it to get 1, and then goes into the 'JMP .' infinite loop (I assume . means 'this address'.

So, our two types of RAM - the 32kwords of panel RAM (so named because it is intended for storage of programs that replace the not-present switch panel in this embedded PDP-8) are overwriting the 32kwords of main RAM. Why?

The HD-6120 datasheet says the CPU pulls /LXMAR low to latch the address registers for main memory, and pulls /LXPAR low to latch address registers for panel memory. Bob Armstrong's MEM GAL does things a little differently - /LXMAR gets run to one of the RAM address lines directly - so main RAM (/LXMAR low) is 1/2 of the RAM chips, and panel RAM (/LXMAR high) is the other half:

But where does that LXMAR signal come from. On the CPU sheet, there is no output to a global net:

And, therein lies the problem. I copied the original schematic pretty exactly into KiCAD, including this lack of a global net connection where /LXMAR is generated at the CPU. Apparently the software Bob Armstrong used considered all labels to be global and hooked everything up properly - but KiCAD did not, so we ended up with 2 nets:

-/LXMAR going from the CPU to the MEM GAL
-/LXMAR going from pin 31 of 1 RAM chip, to Pin 31 of the other, and to J4 of the Expansion connector.

To get the board up and running, the two need to be connected. I recommend running a jumper on the underside of the board from Pin 4 of the MEM GAL to Pin 31 of the nearest RAM chip, like so:

With this fix in place and the 're-arranged' ROM files provided by Will above, I get a good bootup to the BTS6120 ROM monitor prompt, can list the Help on all of the monitor commands, etc!!

Yay!!

File Attachments
1) HANG.png, downloaded 1226 times
2) LXMAR-RAM.png, downloaded 1203 times
3) LXMAR-CPU.png, downloaded 1168 times
4) Prototype-Fix.JPG, downloaded 1214 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Fri, 29 Apr 2016 08:49:22 GMT
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Andrew -- good catch! Thank you for showing us how you figured out the problem, that logic analyser looks like a really useful tool to have.

I now have all the parts except for the PCB and the HD6120, both still somewhere in the postal system...

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Fri, 29 Apr 2016 10:38:53 GMT
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On the subject of GALs: they come in a B, C or D version. I've been looking through the Lattice datasheet, but aside from a marginal difference in max clock speed and maybe some packaging options I can't find a real difference. What am I missing?

RHK

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Fri, 29 Apr 2016 10:53:16 GMT

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PCB has arrived! Only outstanding part is now the HD6120 IC, last seen three days ago in ShenZhen.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Fri, 29 Apr 2016 12:33:54 GMT
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I can confirm that the original Dialight 5554403F ("LED 2MM QUAD 5V YELLOW", DigiKey part 350-1798-ND) fits the PCB footprint and that there is plenty of space to install a wire jumper in place of the current limiting resistors. It's quite a small part.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Fri, 29 Apr 2016 15:15:26 GMT
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will wrote on Fri, 29 April 2016 05:33I can confirm that the original Dialight 5554403F ("LED 2MM QUAD 5V YELLOW", DigiKey part 350-1798-ND) fits the PCB footprint and that there is plenty of space to install a wire jumper in place of the current limiting resistors. It's quite a small part.

Sweet.

Current list of updates for v1.0:
1. Connect 2 /LXMAR nets (add global net output for /LXMAR on CPU page of schematic)
2. Fix ROM address line order (probably swap RAM lines to match too just for OCD-ish reasons)
3. Add jumper+PTCC fuse to feed VCC to IDE pin 20 for CF card adapters.
4. Move RAM chip footprints a little bit away from the ROM chips (no room for inserting a chip puller if you want to remove the chips!)

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 30 Apr 2016 22:40:01 GMT
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OS/8 is up and running! I transferred the images linked on http://www.sparetimegizmos.com/Hardware/SBC6120_Builders.htm via the ROM Monitor 'DL' command per the kermit instructions in the SBC6120 User's Guide. This takes about 3 hours per image. The main OS/8 image goes to partitio 0 ('DL 0000') and the OS/8 Games went to partition 1 ('DL 0001')

Somehow I've ended up with no working CF card reader since my digital cameras all use SD cards now. I've got one on the way - at which point I can make an image files that could be written with win32diskimage/dd, which will be a much faster way to get started.

Note that the serial port settings for the ROM Monitor and OS/8 are, annoyingly, different. The monitor wants 8N1 and OS/8 is 7N1. So when you use the 'B' command in the monitor to start OS/8, you then have to change your serial terminal settings to match.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sun, 01 May 2016 15:55:01 GMT
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Andrew

May I suggest another update for v1.0:
- Clearly mark the polarity of C29, C30, C31, C32, C37.

PS my board is now fully assembled and programmed including the fixes and IDE power PPTC; just waiting on the HD6120 CPU to arrive in the post.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by jcoffman on Sun, 01 May 2016 17:35:40 GMT
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Will,

Polarity is clear. Square pad means pin 1, which is always the + lead. After your comment, I buzzed the board. It is correct.

Markings on small capacitors are sometimes hard to read. I like the convention on caps to have pin 1 the longer lead. Also true on many LEDs.

--John

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sun, 01 May 2016 18:02:08 GMT
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Thanks; I similarly buzzed it out with a printed copy of the MAX232CPE datasheet in hand just to be sure.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Mon, 02 May 2016 00:29:43 GMT

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Alive!

Built up the board tonight, with the scrambled .rom files and the jumper wire correction.

Booted right up into OS-8, played adventure.

Then swapped the 5mhz oscillator for an 8mhz oscillator without any problems (and a very noticeable boost in speed).

Kudo's to Andrew for getting the board designed and working (and to Will for scrambling the Roms).

One more suggestion, add a small connector in parallel with the reset switch, so a case mounted switch can also be used.

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Mon, 02 May 2016 07:19:28 GMT
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The manual warns about the speed of the 82c55:

"You must use at least the 5 MHz version of the 82C55 (as indicated by an A5, or -5 suffix); slower
parts will not work."

Will the IDE still work at 8MHz?

RHK

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 02 May 2016 11:02:35 GMT
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Gary - brilliant to hear that another board is up and running! Brings me hope that mine will work once the HD6120 arrives on the slow boat from China.

Quote:One more suggestion, add a small connector in parallel with the reset switch

I believe this facility is provided for on the board already. One of the test points (TP3, from memory) can be pulled to ground through an external switch in order to reset the system. It could be improved by changing it from a single test point to 2-position header with the second position being wired to the ground net.

Quote:Will the IDE still work at 8MHz?

The Intersil CP82C55AZ I have fitted on my (unproven) SBC6120-RBC board is rated at 8MHz. I have the same chip on my Zeta2 and KISS-68030 MF/PIC boards which all run significantly faster so I am expecting it will work fine.

Did anyone else get caught out by the 0.1" decoupling cap lead spacing? I am so used to using 0.2" lead spacing for these parts that I just assumed it would be 0.2" and I could use the huge stock of these I have already. Not a huge problem, just took 15 minutes with some flat nose pliers to reshape the leads appropriately.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Mon, 02 May 2016 11:12:47 GMT
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Bob had mentioned in his documentation that most HD1-6120's run fine at 8mhz, and in my experience the IDE works nicely at that speed.

Agree - the test points have both reset and ground, but they don't make for a "clean" hookup. A small 2 position connector would be easier to use if there is space.

I had a large batch of 0.1uf caps that I've been re-bending to 0.2" spacing, so for me it was a pleasant surprise

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Mon, 02 May 2016 13:34:51 GMT
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Oh, goodie. I assume it is just a pulse rise time issue then, with the 82C55. I can't find a suitable 5 MHz oscillator anyway. I know Digikey sells them, but they also charge a $46.00 - $58.00 shipping fee. I have 4, 4.9152, 6 and 8 MHz. So I'm good.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 02 May 2016 19:24:45 GMT
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I went to scan a document today, and found on my scanner an SBC-6120-RBC Edition prototype board!

The board house must have sent me 6 boards for the price of 5, and I missed it in my excitement.

If anyone is interested in this last prototype board - given the knowledge of the 'scrambled/re-arranged ROM' problem and the single jumper wire being needed - it is available.

I'd like to wait for Will, John, and Wayne to get their prototypes built to collect any further feedback before a final run, as well as making a really spot-on Wiki page - so it may be a couple of months before we see the final version.

I think either Gary or Wayne mentioned having the original STG FP6120 front panel board as well, I'd be interested in testing the RBC Edition with that as well.

Current list of updates for v1.0 - getting into the detailed ones now:
1. Connect 2 /LXMAR nets (add global net output for /LXMAR on CPU page of schematic)
2. Fix ROM address line order (probably swap RAM lines to match too just for OCD-ish reasons)
3. Add jumper+PTCC fuse to feed VCC to IDE pin 20 for CF card adapters.
4. Move RAM chip footprints a little bit away from the ROM chips (no room for inserting a chip puller if you want to remove the chips!
5. Add a 2-pin connector for case reset button (modify existing test point near the reset switch)
6. Try routing the board with the IOT2 GAL rotated to match the direction of the other chips on the board (this has caught me up a couple times, was an artifact of the original hand-routed board, maybe Freerouting can do better)
7. Mark the net between the Molex connector and the fuse as a 2x width trace in Freerouting to be consistent with the other VCC/GND traces being 2x width - (VCC comes out of the fuse)
8. Add a 'Square pins positive' text note near the MAX232 polarized caps. This will be more readable than tiny plus signs while still providing a visible reminder on the board itself
9. Update text next to J15 - BTS2160 ROM monitor code is now too large for a 27C64 or 28C64, so 27C256 or 28C256 are required. No sense in calling out a part number that won't work on the silkscreen.
10. Draw in simple silkscreen outlines for the Molex power connector and the power switch

Guys - one other thought I have had is to go to the smaller floppy-type Molex power connector.

Edit: Also, I like to use the Ti MAX232N's on my boards, they are ~0.59 vs ~$2.60 for the Maxim parts.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 02 May 2016 19:34:28 GMT
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Point 7 (wider trace Molex->fuse) -- I view this thin link as a backup fuse :)

Floppy-type Molex power connector -- YUCK, no thanks.

If you're looking to change/supplement the power connection options how about adding a 6-pin header like the one used on the 4UART-USB board. This could supply power as well as serial at TTL levels (with presentation over USB at the host end). One could then omit the MAX232 entirely. Alternatively a jumper could allow the builder to switch the UART RX line input between the 6-pin TTL serial header and the MAX232 receiver output pin.

W

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Mon, 02 May 2016 21:24:50 GMT
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Could just forget the MAX232 1uf caps and use 0.1uf caps which are fine with most current xx232 variants. I've used the HIN202CPZ recently.

I'd vote to leave the IOT1 reversed, only so that all of the boards look the same

My front panel is in a sealed up case, so testing it with this board will be a bit of a project. If Wayne's is more accessible I'll hold off.

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by jcoffman on Mon, 02 May 2016 23:05:15 GMT
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Please, please do not change the power connector. The 3.5" floppy connectors are loose and slip easily on boards on the workbench. The larger hard drive connectors connect very solidly, and stay connected.

BTW: the Molex pin dia. is 60 mils, as on this board. Many similar connectors use a 70 mil pin diameter, such as the connectors used on the SBC v2, SBC-188, Z180 MarkIV, and all Backplanes.

--John

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Tue, 03 May 2016 12:42:02 GMT
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My original SBC6120 and front panel are easy to play with. I will definitely be testing it as soon as possible. Currently out of the country, so I need a bit more time to get my new board built.

Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 04 May 2016 01:03:44 GMT
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Working Prototype Eye Candy:

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 04 May 2016 04:46:07 GMT
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Sweet! I have a whole bunch of pictures of mine all through construction that I will post in a 'Prototype' gallery on the wiki.

This has gone pretty smoothly.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 04 May 2016 11:43:53 GMT
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Well, my HD1-6120-8 CPU arrived this morning. I literally hugged the (somewhat surprised) postman.

Dropped it in the board and, hmmm. No joy.

What I get is:
- no output on serial port
- on the quad LED display, leftmost LED (power light) illuminates all the time.
- on the quad LED display, rightmost LED illuminates apparently instantly after reset.
- NO binary countdown ie 7, 6, 5, 4, 3, 2, 1 as the manual suggests. Just direct to 1.

If I hold down the reset button the power LED remains lit but the rightmost LED goes out. When I release the reset button the rightmost LED lights up immediately.

If I remove the CPU clock crystal and repeat the test, the rightmost LED never illuminates.

Hmmmmmmm. Any suggestions?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 04 May 2016 11:49:12 GMT
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Ah. I had the ROM jumper set incorrectly Whoops! Now it does the countdown and then the ROM Monitor text appears on the terminal. Phew.

Oddly if I hit a key on the terminal it seems to repeat indefinitely. IE hitting "a" once I get a row of "aaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa" presumably until the input buffer is full. If I hit Enter I get ">" prompts scrolling off the screen continuously....

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 04 May 2016 14:40:39 GMT
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Looking at the schematic, I wonder if U11 is faulty. These are second-hand GALs and I know at least one in the batch had a fault.

U11 pin 16 is "CLR KEYBOARD FLAG L", pin 10 is "KEYBOARD FLAG H". A fault on either of those would give the observed behaviour.

I will program a replacement this evening and try swapping it out to see if it cures the observed issue.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 04 May 2016 16:04:12 GMT
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Programmed replacement U11, problem gone. Schematics for the win!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 04 May 2016 21:32:42 GMT
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Serial port settings -- I feel I must be missing something!

As far as I can tell the ROM monitor expects 8 bits data, no parity, 1 stop bit. But it seems OS/8 expects 7 bits data -- not sure about parity, and I assume 1 stop bit.

Rather tedious to reconfigure the terminal each time. Have I missed some trick here?

Subject: Re: New Board Development - SBC6120-RBC Edition

Posted by Andrew B on Wed, 04 May 2016 21:35:26 GMT
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Nope, that's the way it works. Kind of annoying.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 04 May 2016 21:46:14 GMT
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>Nope, that's the way it works. Kind of annoying.

Hmm, might be worth patching the ROM to have it use 7-bit mode too. I suppose that would prevent the binary file transfer functions from working. But with easily swappable CF cards I am not sure I would ever use these functions anyway.

Is 7E1 the correct setting?

PS I am now running at 8MHz with no apparent issues (using HD1-6120-8 CPU, CP82C55AZ).

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 04 May 2016 21:48:46 GMT
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I've used 7N1 so far, but 7E1 might be the actual setting.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 04 May 2016 22:45:08 GMT
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7, Mark, 1 is correct iirc. Monitor works well enough with this setting to boot OS-8, but never used it for much else.

Your GAL issue may well be the TL866, I found that it really is not reliable with 22V10's. Some would program but not work in my experience. Also some would program but then seem to be damaged afterwards.

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by jcoffman on Thu, 05 May 2016 03:28:16 GMT
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I received the last of the components today and I have the board fully populated. It is hanging at POST 5 -- ROM checksum error. I've checked the actual ROMs (Will's scrambled versions) and re-programmed the MEM GAL so far. I haven't checked the IOTx GALs, which are recycled from the KISS-68030 project. I really have no reason to suspect them. The LXMAR circuit correction is installed.

Would it be possible to get some schematics of the actual board I am working with? Either the Kicad .sch files or some .pdf files generated from them.

--John

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 05 May 2016 06:07:30 GMT
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Attached .pdfs of the schematic and the board.

(Once we have a v1.0 w/all the fixes, I will post the full KiCAD files on the Wiki; files with issues don't seem very useful to anyone.

File Attachments
1) SBC6120-RBC-0.99.pdf, downloaded 494 times
2) SBC6120-RBC.pdf, downloaded 394 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Thu, 05 May 2016 12:03:56 GMT
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Looking for software to run on this machine; the common distribution format seems to be images of various standard DEC media types. The SBC6120 seems to use 2MB long "partitions" with every 12-bit word stored in two bytes (four bits unused).

Any suggestions for software to read/write OS/8 format filesystems, or to convert the DEC media images into something I can write onto my compact flash card? Or even documentation of the format(s) so I can whip up my own converter tool?

Thanks

Will

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by pbirkel on Thu, 05 May 2016 12:36:55 GMT

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IMO this is the type of question better targeted at users of the original SBC6120 ... on the STG mailing list ;->.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 05 May 2016 15:08:49 GMT
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There is a list of useful utilities across different websites at the bottom of this page - http://www.tronola.com/html/building_the_sbc6120-fp6120_pa2. html

The PDP-8 spanned many years so a lot of the images out there are for software that pre-dated OS/8, so it's just a single piece of software on a paper tape using the BIN loader or whatever. I have to admit that I'm not super familiar with that stuff.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Thu, 05 May 2016 15:47:57 GMT
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OK I think the solution here is probably to port FLX8 to Linux. I'm on it, like a bonnet.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 05 May 2016 19:05:36 GMT
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I moved the front panel discussion to https://www.retrobrewcomputers.org/forum/index.php?t=msg&amp ;th=60&start=0& so the debugging/software stuff on the existing prototype boards is easier to follow.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Thu, 05 May 2016 20:15:41 GMT
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Attachment is a quick and dirty port of FLX8 that builds and runs on Linux. Not well tested yet. I've transferred a few files with it. It can read SBC6120 disk images (use "MOUNT <filename> /ID"). It appears to support RK05, RX01, RX50 formats as well but I've not yet tested those.

Commands appear to match those for FLX-W32 as described here:

MOU.NT <file or device> [/RX01][/RX50][/VM.01][/ID.01][/RK.05]

[/PHY.SICAL][/VIR.TUAL][/READ._ONLY][/SYS.TEM]
[/INI.TIALIZE][/NOCONF.IRM]
DISM.OUNT
PART.ITION <number>|<letter>
DU.MP <block>
DIR.ECTORY [<file(s)>][<output dev>][/BRIEF][/FULL]
TY.PE <file(s)>[/CONF.IRM]
REA.D <file(s)>[<dest file(s)>][/SYS.TEM][/CONF.IRM][/BOOT]
[/IM.AGE][/AS.CII][/BY.TE]
REN.NAME <oldfile(s)> <newfile(s)>[/CONF.IRM]
DEL.ETE <file(s)>[/CONF.IRM]
WRI.TE <file(s)>[<dest file(s)>][/SYS.TEM][/CONF.IRM][/BOOT]
[/IM.AGE][/AS.CII][/BY.TE]
ZER.O [/SYS.TEM][/NOCONF.IRM]
Q.UIT / EX.IT

File Attachments

1) flx8-linux.tgz, downloaded 423 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by jcoffman on Thu, 05 May 2016 20:21:27 GMT
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Board update may be required by EPROM users. Pin 1, Vpp, is left floating. This is okay with some manufacturers; others require that Vpp be held at Vss or Vcc during normal operation; and still others require Vpp to be held at Vcc during normal operation. This was eliminated as not causing the problem I have seen, but may affect someone in the future. Anyhow, tying pin1 and pin32 together did not affect what I am seeing.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 05 May 2016 20:51:22 GMT
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I'd take a close look at the /LXMAR fix - if it's failing where it is in the monitor code, then it has already done a very basic check of memory and started copying over the ROM contents to RAM. It's weird that the checksum would fail there unless what is read back isn't what is in the ROM.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by jcoffman on Fri, 06 May 2016 00:51:23 GMT
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Code executing from ROM seems to be okay. My EPROM is salvaged from an ancient PC. Nice and slow. But the other GALs are leftovers from the 68030 project, and are very fast, as is the

new SRAM. I think the contents written to RAM are not reading back correctly because the TRH (read hold time) is not being satisfied. I have some slow GALs on order now.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Fri, 06 May 2016 04:24:10 GMT
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The 6th prototype board has been claimed by another intrepid builder.

Quote:Code executing from ROM seems to be okay. My EPROM is salvaged from an ancient PC. Nice and slow. But the other GALs are leftovers from the 68030 project, and are very fast, as is the new SRAM. I think the contents written to RAM are not reading back correctly because the TRH (read hold time) is not being satisfied. I have some slow GALs on order now.

Considering that the original STG design used even faster SRAMs (4-bit wide cache RAMs at 25, 35, and 45 ns) - I'd be surprised if the GAL being faster (7.5ns vs 15ns? impacts the SRAM - at 5mhz I believe there should almost be an entire 200ns clock cycle for the data to become valid before it is read by the CPU.....

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Fri, 06 May 2016 08:06:46 GMT
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John

I am using 15ns ATF16V8B and the same 7ns GAL22V10C parts that I used on the KISS-68030. RAMs are 55ns AS6C1008 and ROMs are 150ns AT28C256. Works at 5MHz and 8MHz CPU clock.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Sat, 07 May 2016 23:37:24 GMT
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My board is up and running -- at least to the monitor anyway. Out time today, but will proceed with testing IDE and then front panel hopefully tomorrow.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sun, 08 May 2016 13:36:03 GMT

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Andrew -- another minor modification that might save some board space: Change the six/seven 10K resistors for a bussed resistor network.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Sun, 08 May 2016 22:04:04 GMT
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My IDE interface is working great.

I connected to my existing FP6120 front panel. Basically works, but seeing an odd behavior I can't explain. The bottom row of lights only works when the rotary switch is in the "MD" position. This anomaly occurs when running OS/8 as well as Steve Gibson's Deep Thought code (which I believe addresses the lights directly). The bottom row of lights simply do not illuminate at all unless the rotary switch is in the "MD" position. However, once lights are lit, they will stay lit even if rotary switch if moved to non-MD position.

I have confirmed I can swap back to my original SBC6120 CPU board and the bottom row of lights works correctly.

Obviously, this could be a build problem, but not sure what to check offhand...

Top row of lights and switches all seem to be working perfectly.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 08 May 2016 23:22:15 GMT
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Okay, well we've got 4/5 boards up and running so far.

Let's see if we can figure out this FP6120 thing.

The rotary switch position and bottom row of lights are controlled by software in the ROM. A 30hz interrupt signal generated by the 555 timer sends the CPU into the corresponding code to update the lights based on the rotary switch position....

One thing I noticed is that my v271 ROMs from my Spare Time Gizmos kit (dumped using my EEPROM programmer) are not byte-identical to the v271 ROMs in the .zip file that Gary dug up on his hard drive. Maybe the difference impacts the function of the rotary switch somehow???

OR I screwed up the expansion connector wiring somehow - the top lights run directly off the memory address lines, the bottom lights are latched off the data lines, so if I made a schematic error it could impact only those bottom lines.

Andrew

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 09 May 2016 05:35:09 GMT
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Wayne - which files did you use to program your GALs?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Mon, 09 May 2016 15:33:22 GMT
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I am using Atmel PLDs and programmed them from the latest design archive I found on the Spare Time Gizmos website. I have attached a zip file of the .JED files used. There are also PLDs on the front panel -- those are "as supplied" by Bob Armstrong.

One interesting factoid is that the ROMs on my original SBC board as supplied by Bob Armstrong are v320. I forget why, but have the impression that the v320 ROMs were a branch from older ROMs to support the IOB6120. Indeed, on startup, the v320 ROMs look for an IOB6120 and report that it is not found. I would love to see/compare the source for v320 with v271, but have no clue where to find v320 source. Give me a little time and I will extract the v320 binaries and run them through Will's scrambler and try them to see if that makes any difference.

I will also mention that I am seeing some unreliable startup behavior from the RBC SBC board when connected to the front panel. Let me be a little more specific. When operating standalone, the RBC CPU board is powered from it's onboard molex connector and starts and operates completely reliably. Startup of the RBC SBC when mounted on the front panel is hit and miss. Sometimes starts fine, but frequently hangs at random places (i.e., the diagnostic lights freeze at different displays). Once the RBC SBC achieves a good startup, it runs fine (aside from the issue with the second row of lights). The unreliable startup behavior is exhibited regardless of whether I am applying power or pressing reset. I will mention that when mounted on the front panel, it is powered via the 50-pin connector which derives it's power from an 12v wall wart power supply running through an onboard regulator. My point is that it could certainly be a power related issue. However, my original STG SBC starts up completely reliably from when mounted on the front panel.

So, I am going to work on the ROMs as time permits. I am open to suggestions on the startup behavior.

-Wayne

File Attachments
1) PLD.zip, downloaded 333 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 09 May 2016 15:41:03 GMT
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Wayne -- the reliability issue you report does sound like a power issue. I note that the power traces to the 50-pin connector are quite thin. Perhaps try soldering a 47uF electrolytic across pins 1 and 2 on J4, on the back of the board, and see if this resolves the issue? Maybe also run some 26AWG from pins 1, 2 on J4 direct to C37.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 09 May 2016 15:46:23 GMT
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The original board was a 4-layer board with internal power and ground planes, so I would not be surprised if it's a power issue. I made all the VCC/GND traces double-width with VCC/GND fill zones added on the top and bottom of the board after running Freerouting, but I did not attempt any hand-routing. You end up with a pretty good fill zone over by the Molex connector that helps send the power all over the board without a lot of resistance, but the expansion connector just has one set of lines and that's it.... I was thinking of going to 2 oz copper for the V1.00 boards.

The v320 ROMS were for the SBC6120-Reduced Cost - http://www.sparetimegizmos.com/wdoc/index.php?title=SBC6120- RC_User_Manual - if you look at the changelog in the v271 sources Gary found, all the IOB integration is already done....

Note: On J4, pins 1/2 are both VCC, and pins 17/18 are GND.

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by jcoffman on Mon, 09 May 2016 17:15:52 GMT
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RE: ailing board

I am at wits end. I have buzzed out the traces on the board one-by-one, IC-pin to IC-pin. No bad connections in sockets; no cold-solder joints; no cracked traces or vias. All of the small chips have been tested or substituted. GALs have been replaced & re-programmed. The JED files compare with Wayne's recent post. So I am down to two possibilities: a). The timing issue I can see from the CPU data sheet (relatively unlikely); or b). a sick CPU. The last is the only chip I cannot substitute or put in a tester.

Waiting for the slower GALs to arrive, and just praying that that is the source of the trouble.

RE: voltage issues

This board does not draw enough power for that to be an issue. I was a little concerned about the voltage drop across the fuse, but the one I am using does not make that a problem. I see a good 5.05v on the chips on my board. Perhaps a larger cap across the 47uf power filter might make a

difference, and it would not do any harm.

--John

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Mon, 09 May 2016 17:18:51 GMT
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The supplemental capacitor sounds like a good idea and certainly would cause no harm -- will try that.

On the ROM versions, yes, thank you, my memory was foggy. It was the RC model that v320 applied to, not the IOB. Still confused about the numbering and why my SBC6120 came with v320 ROMs. I think I will take the opposite approach and put v271 on my original SGT SBC and confirm bottom row of LEDs work.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Mon, 09 May 2016 23:50:21 GMT
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When I put the v271 ROM (non-scrambled) on my original STG SBC, the second row of lights misbehaves. Again, I am saying that the second row of lights (data bits) only work when the rotary is in the MD position. So... this points more suspicion to the v271 image we are using which apparently is not binary identical to the one Andrew dumped from his ROMs.

Thoughts?

Oh, and no joy on the 47uF cap added at the 50-pin power pins. Startup of the RBC SBC is still flaky. I am noticing that startup when the board is cold (has been turned off for a while) seems to be 100% reliable. Flakiness starts after board has warmed up for about 5 mins. I am going to go over all my solder joints just for fun. However, it perplexes me that the flakiness only occurs when attached to the front panel. Voltage at my chips runs between 4.94 and 4.96 which should be OK. Actually, the voltage at my chips when I run without the front panel is ~4.75 due to the fuse that applies in that scenario.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition

Posted by Andrew B on Tue, 10 May 2016 05:11:15 GMT
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Attached is a .zip with the source/hex files for the v320 BTS6120. This is the most recent version.

Also included is a version that has been run through Wills 're-arranger' for the 0.99 prototype boards. I haven't had time to test on my board yet - let me know if this works! Will test tomorrow PM.

File Attachments
1) bts6120_v320_src_hex.zip, downloaded 443 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Tue, 10 May 2016 19:58:45 GMT
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Thanks Andrew. I am running on the scrambled v320 ROMs now. Light behavior does not appear to be fixed by this.

My original CF Card got corrupted somehow, so I am a bit handicapped. But, I can say with certainty that when running CHESS on the STG SBC, the data lights flicker with the rotary set to either MD or AC. With the RBC SBC, the lights only flicker on MD. I switched back and forth between the STG and RBC boards repeatedly to confirm what I was seeing. Obviously, we have not eliminated the possibility of a construction issue on my end.

-Wayne

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by Wayne W on Tue, 10 May 2016 20:08:44 GMT
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jcoffman wrote on Mon, 09 May 2016 10:15RE: ailing board

I am at wits end. I have buzzed out the traces on the board one-by-one, IC-pin to IC-pin. No bad connections in sockets; no cold-solder joints; no cracked traces or vias. All of the small chips have been tested or substituted. GALs have been replaced & re-programmed. The JED files compare with Wayne's recent post. So I am down to two possibilities: a). The timing issue I can see from the CPU data sheet (relatively unlikely); or b). a sick CPU. The last is the only chip I cannot substitute or put in a tester.

John,

In the process of switching from the v271 to v320 ROMs, I wound up using slightly different chips.

I was previously using Xicor X28C256 and am now using Atmel AT28C256. In both cases the chips had a speed rating of 150ns. I need a few more hours to say for sure, but it looks like the AT28C256 chips have improved (possibly fixed) my boards reliability problem. I think you said you originally were using 250ns parts. I wasn't clear from your posts if you have tried different ROM chips. Wonder if you have tried anything else? Especially something faster? When my board was previously failing to start, the most common place for it to get stuck was the ROM Checksum. I need a few more hours to say if my startup reliability is totally resolved.

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by jcoffman on Wed, 11 May 2016 00:06:00 GMT
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The problem with my board is solved. Interesting story today when it magically started to work. At first, two switching power supplies were suspect, since the board seemed to work best off of a little breadboard power supply with a 7805. Hmmm, high frequency ripple on the switching supplies? But the problem returned when I moved out here with that little analog supply and connected to a terminal. Stop at '5'. ROM checksum bad. The same setup works in the back bedroom--on the metal desk. So now I am here on the wooden computer bench, hooked to a terminal, seeing the SBC6120 monitor. The difference: a sheet of aluminum foil underneath all (insulated with thicknesses of paper). The SBC6120 works fine. No chip changes; no new components; no problem with the board or soldering.

For some reason, this board appears to be extremely sensitive to noise, whether background or self generated. It works with the old Apple switching power supply, the little analog supply -- but only if it is sitting above a good ground plane. IT WILL NOT WORK ON A WOODEN SURFACE.

In the process, I added a 1000uF cap between the two test points on either side of the Zener. It works with or without this extra cap. The ground plane is the thing.

[Perhaps there was a reason for the STG board to be 4 layers.]

--John

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by Andrew B on Wed, 11 May 2016 03:07:39 GMT
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Wayne W wrote on Tue, 10 May 2016 13:08
John,

In the process of switching from the v271 to v320 ROMs, I wound up using slightly different chips. I was previously using Xicor X28C256 and am now using Atmel AT28C256. In both cases the chips had a speed rating of 150ns. I need a few more hours to say for sure, but it looks like the AT28C256 chips have improved (possibly fixed) my boards reliability problem. I think you said you originally were using 250ns parts. I wasn't clear from your posts if you have tried different

ROM chips. Wonder if you have tried anything else? Especially something faster? When my board was previously failing to start, the most common place for it to get stuck was the ROM Checksum. I need a few more hours to say if my startup reliability is totally resolved.

Quote:For some reason, this board appears to be extremely sensitive to noise, whether background or self generated. It works with the old Apple switching power supply, the little analog supply -- but only if it is sitting above a good ground plane. IT WILL NOT WORK ON A WOODEN SURFACE.

I've done all of my testing sitting on a wooden desk, with 150ns AT28C256's..... So it seems like overall these prototypes are not super stable, which is unfortunate (and completely on me, since the original design is quite reliable).

One thing John pointed out in an email is that /WE of the EEPROMs should really be pulled HIGH which the board does not do, it leaves Pin 27 of the EEPROM sockets floating with the jumper in the 28C256 position. Wayne, if you intend to use only EEPROMs in your board, perhaps making that modification would resolve the difference you are seeing between the two EEPROM brands/speeds. John also suggested a slick 4-pin jumper arrangement that will make sure we are putting all the pins at the right voltages when switching between 27C256 and 28C256 - which I should have spent more time thinking about and reviewing the different data sheets.

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by Wayne W on Wed, 11 May 2016 03:31:11 GMT
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Andrew B wrote on Tue, 10 May 2016 20:07

I've done all of my testing sitting on a wooden desk, with 150ns AT28C256's..... So it seems like overall these prototypes are not super stable, which is unfortunate (and completely on me, since the original design is quite reliable).

One thing John pointed out in an email is that /WE of the EEPROMs should really be pulled HIGH which the board does not do, it leaves Pin 27 of the EEPROM sockets floating with the jumper in the 28C256 position. Wayne, if you intend to use only EEPROMs in your board, perhaps making that modification would resolve the difference you are seeing between the two EEPROM brands/speeds. John also suggested a slick 4-pin jumper arrangement that will make sure we are putting all the pins at the right voltages when switching between 27C256 and 28C256 - which I should have spent more time thinking about and reviewing the different data sheets.

I don't want to restrict myself to EEPROMs, but I can easily try the Xicor X28C256 EEPROMs with a temporary strap on pin 27 to +5V. I will let you know if that helps.

Regardless, I am definitely finding that switching from the Xicor ROMs to Atmel ROMs has stabilized my board. Now seems to be 100% stable.

-Wayne

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by Andrew B on Wed, 11 May 2016 06:53:24 GMT
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Looking at some datasheets (attached for reference).

Data input from EEPROM to HD-6120, HIGH state:
HD-6120: VIH, Min = 70% VCC => 5.0V*.70 = 3.5V
AT28C256, XC28C256: VOH, Min = 2.4V
(Looks like -1.1V margin on this one?)

Data input from EEPROM to HD-6120, LOW state:
HD-6120: VIL, Max = 30% VCC => 1.5V
AT28C256, XC28C256: VOL, Max = 0.45V
(1.05V margin here)

Data input to EEPROM from HD-6120, HIGH state:
AT28C256, XC28C256: VIH, Min = 2.0V
HD-6120: VOH, Min = VCC-0.5V => 5.0V-0.5V = 4.5V
(2.5V margin here)

Data input to EEPROM from HD-6120, LOW state:
AT28C256, XC28C256: VIL, Max = 0.8V
HS-6120: VOL, Max = 0.5V
(0.3V of margin)

So, just looking at the datasheets for the parts, it seems like we'd likely have susceptibility to the differences between EPROMs and EEPROMs, manufacturer-to-manufacturer variations, and potentially PCB-layout related noise on ROM reads. Most E(E)PROMS will probably output a 'high' signal that is better than their datasheet minimum spec.....but it's not guaranteed. I could definitely see the 4-layer board helping if I am reading these datasheets correctly.

Can one of you guys check and make sure I'm not reading this wrong and totally off base here?

Edit: I think I'm wrong above, because the 'test condition' on the EEPROM data sheets is a current of -400uA on the outputs, while the maximum input leakage current on the HD-6120 inputs is 10uA. So the ROM outputs should end up at a much higher voltage than what is in the datasheet for the test condition. This 27C256 datasheet - http://www.ee.ryerson.ca/~jkoch/data_pdf/27c256.pdf - shows 2.4V at -400 uA, but 4.4V at 0 uA.

Leaving the rest of the post for the datasheets and stuff.

File Attachments

1) X28C256.pdf, downloaded 531 times
2) AT28C256.pdf, downloaded 519 times
3) HD6120_Specifications.pdf, downloaded 651 times

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by will on Wed, 11 May 2016 11:02:54 GMT
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I think on my board I am going to remove J15, join pins 2 and 3 with a wire jumper, and connect pin 1 to VCC with a short patch wire. I am using AT28C256 EEPROMs. All my bench surfaces are wooden.

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by rhkoolstar on Wed, 11 May 2016 12:24:03 GMT
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Andrew,

Pondering the schematics I ran across an anomaly:

The original schematics route the signal INTGNT to CPU pin 2 "INTGNT", however pin 2 on the CPU is "DMAGNT"
You route the signal likewise (although you label pin 2 correctly as DMAGNT), but maybe the original schematics contain a typo and pin 31 should be wired instead.
Maybe check the original board? (I don't own one (yet)

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by gkaufman on Wed, 11 May 2016 14:12:10 GMT
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I missed a bit of this discussion as I was unfortunately out of town.

I used "old fashioned" 27C256 Eproms. AMD AM27C256-205DC with the 271 scrambled code.
Power supply is a junky floppy power cube from Ebay.
No shielding (sitting on a towel on a wood bench).

I'll run it some more tonight, but before I left I played adventure for a while with no glitches.

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by sparetimegizmos on Wed, 11 May 2016 15:34:35 GMT
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A few comments regarding the SBC6120 ROMS which may be helpful -

The PDP-8 numbers its bits from left to right. That's not the modern convention, but you're not building a modern computer. I think you already figured this out the hard way and you can cope with it any way you want, but that's why the address bits on the original SBC6120 were not wired up to the EPROM as you expected.

BTS6120 v320 was for the SBC6120-RC (not RBC) model, but it was fully backward compatible with the original SBC6120. Whenever somebody ordered an SBC6120 I would ship the latest firmware, so whoever got the v320 ROMs in his SBC6120 simply has one of the last production units. There's no mystery there.

There's a build date and time in BTS6120. This isn't a secret - it prints out the timestamp when you boot it. If you reassemble, for example, the v271 source then it's going to get today's date and time and the ROM image you get won't be byte for byte identical to the v271 ROMs I shipped. And as a consequence, the ROM checksums will change as well.

OS/8 really wants 7M1 as the RS232 format - that's what a real ASR33 would have done. Most programs ignore the MSB, so 7E1 also usually works. BTS6120 is perfectly happy with 8N1, 7E1 or 7M1. There's no need to change the terminal settings when booting.

Bob

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by sparetimegizmos on Wed, 11 May 2016 15:41:15 GMT
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Regarding the data LEDs that don't update -

In the MD position, the data LEDs simply display what's on the data bus directly, but in all the other positions the data LEDs are driven by the firmware. The firmware updates the front panel in response to the 30Hz CPREQ interrupts generated by the 555 on the FP6120. If the LEDs aren't updating, my first guess would be that this 30Hz CPREQ is not making it to the CPU.

Bob

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 11 May 2016 16:08:42 GMT
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Thanks for the suggestions Bob. This has definitely been a learning experience. I thought of sitting down with both the original schematic and my schematic with a highlighter and red pen to do a final check, like how I check mechanical drawings at work, but my excitement got the best of me and I just went to fab. Otherwise I would have caught the ROM pinout issue for sure.

On the CPREQ interrupt, I think I figured it out. The orientation of the CPREQ jumper J10 on our boards is reversed from the orientation on the original STG boards.

When the board is being used alone this isn't a problem, but when it interfaces with the FP6120 or IOB6120, the pinout is incorrect.

I have to head to work now but tonight I'll post some pictures of the problem and a fix. It will take cutting two traces and two jumper wires on the bottom of the board to fix.

Wayne - if you check J10 with a multimeter on your STG board and the prototype board and see which pin goes to the adjacent 74HC04 and which goes to the CPU, you'll see what I mean. It's reversed.

Added to my list of fixes for V1.00.

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by jcoffman on Wed, 11 May 2016 16:51:21 GMT
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I checked a number of data sheets, and I see two quotations for output voltages: one when connected to TTL, and one when connected to CMOS. Although the attachment I clipped pertains to an EPROM, I see similar output voltages for other chips, including Flash and EEPROM.

File Attachments
1) TTL-CMOS-output-voltage.jpg, downloaded 1286 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by sparetimegizmos on Wed, 11 May 2016 17:14:38 GMT
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FWIW, when I originally designed the SBC6120 I wanted to make a "modern" PDP-8 - something along the lines of a MicroVAX or LSI-11. I never intended there to be a front panel of any kind, and all the panel functions were in firmware. The form factor of the SBC6120 was designed to mate with a 5-1/4" IDE drive and it was intended to piggyback on top of an HDD. The size of the SBC6120 PC board, the IDE and power connector locations, the 4 pin Molex power connector, and even the location of the five mounting holes, were all designed to mate with an IDE drive. My vision was a drive and SBC6120 stack that you could stick in a little external drive enclosure on your desktop. It would have no controls other than POWER and RESET.

But people really wanted a front panel. I resisted for about a year, but eventually I caved in and designed one. The whole front panel design, including the mechanical arrangement where the SBC6120 mounts on the back of the panel, the whole CPREQ jumper/connector "hack", and the power distribution from the front panel to the SBC6120, is a consequence of the fact that it was all added on to something that was never intended to have it. C'est la vie...

The SBC6120-RC (not RBC) was designed from the beginning to have an integrated front panel. Although it's software compatible, including the same BTS6120 boot ROMs, that machine is electrically and mechanically quite a bit different and is a much cleaner design for that end goal.

Bob

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Wed, 11 May 2016 23:27:26 GMT
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Andrew B wrote on Wed, 11 May 2016 09:08On the CPREQ interrupt, I think I figured it out. The orientation of the CPREQ jumper J10 on our boards is reversed from the orientation on the original STG boards.

When the board is being used alone this isn't a problem, but when it interfaces with the FP6120 or IOB6120, the pinout is incorrect.

I have to head to work now but tonight I'll post some pictures of the problem and a fix. It will take cutting two traces and two jumper wires on the bottom of the board to fix.
Added to my list of fixes for V1.00.

The board patch is straightforward since the two traces involved are on the solder side. I have patched my board and confirmed it fixes the light situation. As far as I can tell, my board is now 100% functional!

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Wed, 11 May 2016 23:45:23 GMT
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Bob,

Thanks for jumping in with help and background -- very useful and interesting. Especially the clarity on the ROM versions -- I was very confused on that. Glad to hear there is a single, current version (v320) that represents the latest for all hardware. Sounds like the SBC6120-RC may be the preferred platform for a front panel, but will leave that to Andrew to sort out. I am happy that I now have a spare SBC6120 equivalent for my front panel.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 12 May 2016 04:47:50 GMT
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I think I'd like to focus right now on taking all of the feedback and tweaks we have found and finishing the schematic/routing V1.00 of this board.

I'm still a bit concerned about the instability that John C. has been seeing so I'd like to get some more feedback on that as well. Maybe some manual routing is in order, or going back to 4 layers.

I do wonder if we should change the name a bit for the final board, since it is so close to SBC6120-RC. I'd be open to suggestions in that respect.

As for the future - I've had a few things in my mind:
-Try out rkoolstar's 'mini front panel' board with panel mount switches and lights. A bit fiddly to build, but gives the builder a large flexibility in light and switch selection.
-Make a version with most of the 74xx logic & GALs replaced with a single ATF1508 PLCC CPLD. (This is a bit selfishly driven by my own desire to learn more about VHDL....
-Use the 8255 PPI IOTs to drive Sergey's ParPortProp board, and write a modified BTS6120 and OS/8 device handlers to use that display and storage (I already have that board built and tested with my Zeta, so just wiring + software). This would also leave the existing console SLU free for other OS/8 uses, and create an interesting mashup with some of our existing boards.
-Make a version like the -RC, but also with the CPLD, and use the freed up space to put the VGA/PS2 console directly onto the board
-Etc

My 'real life' work is going to be a bit busy here for a few months, so anything new will probably need to wait for a lull.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by pbirkel on Thu, 12 May 2016 05:16:55 GMT
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WRT rkoolstar's 'mini front panel' board with panel mount switches and lights, if there's a run of them I'd like "in" for a pair, please. Have an assortment of fiddly-bits on-hand for such a purpose and had been planning to work out my own variant on perfboard. Prepared PCBs are so much nicer!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Thu, 12 May 2016 05:57:40 GMT
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Hi Andrew,

Maybe you missed this:
The board is wired with the DMAGNT signal instead of the INTGNT signal.
The net is called INTGNT but it is connected to the DMAGNT pin on the CPU (pin 2)

DMAREQ (CPU pin 3) is disabled (pulled high)
INTREQ (CPU pin 30) is routed to the expansion connector (pin 9)

IMHO, INTGNT (CPU pin 31) should therefore be routed to the expansion connector (pin 10) instead of DMAGNT

In the original schematics these signals are mixed up, maybe in the original board also?

It looks like these signals are not used in the SCB itself, nor in the front panel board or the RAM disk board. I don't know about the IOBoard.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 12 May 2016 07:05:45 GMT
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I did see your message on this.

I multimeter-ed the circuit on my original STG board, and it's Pin 2 (DMAGNT on the HD-6120 datasheet) that is routed to the expansion connector Pin 10.

I agree with DMAREQ pulled high, DMAGNT doesn't seem to be useful, unless there's something I'm missing about how the HD-6120 works.

Need to think a bit more on what to do for a final revision. Pin 24 is unused on the expansion connector, so maybe I could rename the nets and run /INTGNT to Pin 24 on the expansion connector...

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Thu, 12 May 2016 07:30:35 GMT
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Maybe Bob knows?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Thu, 12 May 2016 07:42:47 GMT
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@ pbirkel: PM sent

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by sparetimegizmos on Thu, 12 May 2016 13:40:09 GMT
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RE: INTGNT/DMAGNT

It looks like this is a mistake in the SBC6120. None of the STG boards use INTGNT so the error made no difference. I don't know if the IOS6120 does - the schematic shows that the pin is connected, but you'd have to check Jim's VHDL to know for sure. I suspect that it's not used there, either, especially since it wouldn't work if it did.

If it was my design I would just fix the mistake and connect pin 31 of the CPU to pin 10 of the expansion connector. It serves no purpose to have DMAGNT there. This is Andrew's baby, though, so it's his choice.

Bob

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by jcoffman on Thu, 12 May 2016 18:17:18 GMT
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Andrew,

4 layers, although it doubles the production cost, would probably solve the problem I see. I assume I have some component that is very sensitive to signal ringing. That is probably what the foil under-layer reduces, since it should reduce trace inductance. I am surprised to see any problem on a board that I ran as slow as 3.58mHz. BTW: with the foil under-layer, the board is good at 8mHz.

Somewhere in the back of my mind I think I read a caution with CMOS about its high capacitance, and that switching causes large current transients. Relatively narrow traces distribute power on this board, but I would think that any bouncing of the power supply would be offset by the power & ground zones. Maybe some extra decoupling (electrolytic) on the ROM side of the board would help. Something to try.

Perhaps, also, the trouble I see is just a fluke with the particular CPU I have: Intersil HD1-6120-8, but I believe Will is working with the same CPU.

--John

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Fri, 13 May 2016 03:20:16 GMT
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I took a look at the VHDL code for the IOB6120 (on http://www.jkearney.com/sbc6120/iob6120.htm), and the Pin 141 (INTGNT) is referred to in only 3 places.

Entity Definition:

```
entity iob is
 port
 (clk_in: in std_logic; -- 29.4912 MHz

 -- CPU bus interface
 cpu_ioclr_n : in std_logic;
 dx : inout std_logic_vector(0 to 11);
 clk_write_n_raw : in std_logic;   -- async
 cpu_read_n : in std_logic;
 cpu_sr_read_n : in std_logic;
 cpu_sr_write_n : in std_logic;
 clk_lxdar_n_raw : in std_logic;   -- async
 cpu_c0_n : out std_logic;
 cpu_c1_n : out std_logic;
 cpu_skip_n : out std_logic;
 cpu_intreq_n : out std_logic;
 cpu_intgrnt_n : inout std_logic;
 cpreq_n: inout std_logic;
```

Pin definition:

```
attribute loc of kb_clk : signal is "P138";
attribute pullup of kb_clk : signal is "yes";
attribute loc of kb_data : signal is "P133";
attribute pullup of kb_data : signal is "yes";
attribute loc of lpt_ack : signal is "P91";
attribute loc of lpt_busy_n : signal is "P121";
attribute loc of lpt_data : signal is "P66 P63 P59 P56 P51 P43 P47 P38";
attribute loc of lpt_ddir : signal is "P28";
attribute loc of lpt_error : signal is "P137";
attribute loc of lpt_init : signal is "P7";
attribute loc of lpt_paper_end_n : signal is "P136";
attribute loc of lpt_select_in_n : signal is "P124";
attribute loc of lpt_strobe : signal is "P10";
attribute loc of reprogram : signal is "P85";
attribute loc of rxd : signal is "P23 P26 P27";
attribute loc of txd : signal is "P11 P21 P115";
attribute loc of vga_hs : signal is "P117";
attribute loc of vga_rgb : signal is "P99 P126 P120";
attribute loc of vga_vs : signal is "P102";
attribute loc of cpu_intgrnt_n : signal is "P141";
attribute loc of cpreq_n : signal is "P113";
```

And one line that sets it to High-Z state:

```
  ------------------------------------------------------------ ----------------------------
-- utility and shared logic
  ------------------------------------------------------------ ----------------------------

cpu_intgrnt_n <= 'Z';
```

Based on this, I don't think the IOB6120 uses the signal either. Correcting the error and hooking up the correct CPU pin makes the most sense to me.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Fri, 13 May 2016 03:30:04 GMT
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Updating my list of items to fix for V1.00

Outstanding:
9. Draw in simple silkscreen outlines for the Molex power connector and the power switch

Maybe:
13. Manually route the decoupling caps to each IC to keep from making large loops on the board that might cause noise

DONE:
1. Connect 2 /LXMAR nets (add global net output for /LXMAR on CPU page of schematic to get KiCAD to hook them up)
2. Fix ROM address line order (probably swap RAM lines to match too just for OCD-ish reasons)
3. Add jumper+PTCC fuse to feed VCC to IDE pin 20 for CF card adapters.
4. Move RAM chip footprints a little bit away from the ROM chips (no room for inserting a chip puller if you want to remove the chips!)
5. Add a 2-pin connector for case reset button (modify existing test point near the reset switch)
6. Mark the net between the Molex connector and the fuse as a 2x width trace in Freerouting to be consistent with the other VCC/GND traces being 2x width - (VCC comes out of the fuse)
7. Add a 'Square pins positive' text note near the MAX232 polarized caps. This will be more readable than tiny plus signs while still providing a visible reminder on the board itself
8. Update text next to J15 - BTS2160 ROM monitor code is now too large for a 27C64 or 28C64, so 27C256 or 28C256 are required. No sense in calling out a part number that won't work on the silkscreen.
10. Update J15 to be a 2x2 pin connector so that we end up with the unused pins (Either Vpp or /WE) properly pulled to VCC
11. Switch orientation of CPREQ connector to match STG board
12. Connect Pin 10 on J4 to INTGNT/Pin 31 on CPU
13. To be consistent with other RBC boards KiCAD/Freerouting rules - use smaller DIP pads (to allow two traces to fit through if required), larger power/GND traces, and larger signal and power/GND vias

---

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by jcoffman on Sat, 14 May 2016 20:31:15 GMT
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The origin of the problem with the board needing the Al-foil insulated plane in order to run has been located. The culprit was the 74ACT373's from my parts cabinet. I have used these chips to drive LEDs before, they are compatible with all CMOS logic, and were readily available. 74ACT logic is very fast, and has a very high current drive both sinking and sourcing. Either they switch too fast, or they pull high power supply transients, or both, but changing to 74HC logic eliminates the need for the foil plane.

Andrew: I'd like to send you these chips to see if you can reproduce the problem on another board. You may have better equipment than I for seeing why they cause such a problem. Power distribution & decoupling?

--John

Subject: Re: Front Panel for the SBC6120-RBC Edition
Posted by Andrew B on Sun, 15 May 2016 05:06:33 GMT
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Interesting. You can send me the chips, but while I do have the 16-channel digital logic analyzer - I lack a plain old analog oscilloscope which is probably what will be best for diagnosing this. I'd like to put them in my board and see if they do the same thing though.

Hopefully with more careful routing of the decoupling capacitors and 2 Oz copper vs 1 Oz in the prototypes, we can keep V1.00 a two-layer board.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by djones60 on Thu, 19 May 2016 15:52:48 GMT
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I just ran into this forum thread and have been playing catch up. Sounds like you guys have been doing a lot of great work. If you do another run of these boards, I'd be interested. Especially interested in the programming of the GAL's with the TL866 programmers since I have one of those. I always had my doubts as to if it could program them right or not. Ended up getting an old Needham programmer just in case.

David Jones

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 19 May 2016 15:57:21 GMT

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I'm trying to get a house sold, so not as much time for this as I would like right now.

Hopefully should have a V1.00 out for people to review soon.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by djones60 on Thu, 19 May 2016 16:16:01 GMT
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Sounds great. No hurry. I've too many other projects waiting for my attention as it is! When you get that far, you might want to post something in the Spare Time Gizmos yahoo group. I'm sure there would be interest there. At least, that's where I'd been looking before I ran into it here. Sort of funny, I started out looking for info on the original, pre v4, 8 slot s-100 backplane and seen this:)

Hope things go well getting the house sold.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 19 May 2016 16:39:29 GMT
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Will definitely post to the Yahoo group - I wanted to make sure I had working boards with no showstoppers before I did.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 21 May 2016 23:58:27 GMT
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John sent me his problematic 74ACT373 chips. I was able to reproduce the same POST hang behavior on my RBC Edition board. The original STG board is unaffected and works fine with the ACT chips.

I made smaller and smaller foil sheets and put them under 2 sheets of printer paper under my board. Shielding just the area under the MEM GAL and the 2 '373 chips was sufficient to make the board boot.

I soldered an additional 0.22uf decoupling cap directly between VCC and GND on the back side of the board under the 2 '373 sockets. This fixed the issue (RBCE board boots with no problems with the ACT chips and no nearby shielding).

One drawback to the way I did the prototype boards was that Freerouting routed the decoupling caps "however it wanted", instead of routing them to each adjacent IC. This potentially reduces the effectiveness of the decoupling caps in actually doing their job, and may actually make things worse by creating large 'loops' on the board that act as antennas. (See https://www.fairchildsemi.com/application-notes/AN/AN-389.pd f for a good discussion of decoupling)

I plan to keep the V1.00 boards as a 2-layer board, with the following modifications in the copper routing process:
-Based on feedback from John C. on KiCAD/Freerouting settings that have been using on boards such as the KISS-68030 board:
--Use larger vias for signal traces
--Use larger trace width and larger vias for VCC/GND traces
--Slightly reduce the DIP pad diameters (to match the older RBC boards; the new KiCAD libraries have larger pads on the chips) to allow 2 traces to be routed between each set of pins if required
-Hand-routed decoupling cap connections for the '373 chips to address the stability issue
-*Possibly* hand-routed decoupling caps for all the other chips, if it doesn't make the rest of the board too hard to route (will try both ways)

I will also fabricate the boards with 2oz copper instead of 1oz copper, which should further improve the VCC/GND distribution.

I don't recommend logic family substitution on this board, but I am taking the fact that the ACT chips only caused a problem on the RBC Edition board as an indication that I need to in general improve the VCC/GND paths and more closely couple the decoupling caps.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Thu, 26 May 2016 14:10:51 GMT
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Hi Andrew,
A few suggestions wrt kicad:

- You can use a bus for different signals. Just add a second global label to the bus. ie. an MA[11..0] label and an EMA[2..0] label, both attached to the same bus.

- decoupling may be more effective if you mount the caps under the chips. You will need to use sockets for that off course. I experimented with custom footprints, where two pads were added, 0.05" to the middle, next to (and overlapping with) the power pads, with the same number as said pads.

You can then mount axial caps inside the sockets. You need the turned pin version socket for that and you maybe need to make slight modifications to make room for the cap. Alternatively you can

use sockets with pre-mounted caps (when available).
This solves the long power traces problem, creates more space on the board and simplifies routing.
And you can remove the caps from the schematic

success with selling your house.

File Attachments

1) output.png, downloaded 919 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 05 Jun 2016 02:12:50 GMT
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All, here is where the V1.00 boards stand right now:

Andrew B wrote on Thu, 12 May 2016 20:30Updating my list of items to fix for V1.00

Outstanding:
9. Draw in simple silkscreen outlines for the Molex power connector and the power switch

DONE:
1. Connect 2 /LXMAR nets (add global net output for /LXMAR on CPU page of schematic to get KiCAD to hook them up)
2. Fix ROM address line order (probably swap RAM lines to match too just for OCD-ish reasons)
3. Add jumper+PTCC fuse to feed VCC to IDE pin 20 for CF card adapters.
4. Move RAM chip footprints a little bit away from the ROM chips (no room for inserting a chip puller if you want to remove the chips!
5. Add a 2-pin connector for case reset button (modify existing test point near the reset switch)
6. Mark the net between the Molex connector and the fuse as a 2x width trace in Freerouting to be consistent with the other VCC/GND traces being 2x width - (VCC comes out of the fuse)
7. Add a 'Square pins positive' text note near the MAX232 polarized caps. This will be more readable than tiny plus signs while still providing a visible reminder on the board itself
8. Update text next to J15 - BTS2160 ROM monitor code is now too large for a 27C64 or 28C64, so 27C256 or 28C256 are required. No sense in calling out a part number that won't work on the silkscreen.
10. Update J15 to be a 2x2 pin connector so that we end up with the unused pins (Either Vpp or /WE) properly pulled to VCC
11. Switch orientation of CPREQ connector to match STG board
12. Connect Pin 10 on J4 to INTGNT/Pin 31 on CPU
13. To be consistent with other RBC boards KiCAD/Freerouting rules - use smaller DIP pads (to allow two traces to fit through if required), larger power/GND traces, and larger signal and power/GND vias

Decided not to do:
13. Manually route the decoupling caps to each IC to keep from making large loops on the board that might cause noise

An initial run in Freerouting is looking like we will have < 60 vias which is pretty good!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Sun, 05 Jun 2016 13:45:52 GMT
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Looks good to me Andrew. Covers everything that I encountered.

When routing, suggest you uncheck "restrict pin exit directions" in Route Parameters of FreeRoute. It will result in somewhat cleaner routing of traces to pads (a trick John passed on to me).

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 05 Jun 2016 15:57:24 GMT
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Thansk a ton Wayne, that was my last annoyance Freerouting was the way it was routing into pads seemed to be a bit oddball and take up more space than needed!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by davetypeguy on Mon, 06 Jun 2016 19:06:27 GMT
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Hurray! I was able to finish the "6th" of the 5 prototype boards over the weekend. I installed the jumper fix on the back, and finally received the missing part I was waiting on (vendor shipped the wrong chips and had to replace them). I had issues with the terminal acting up, but after reading Will's description of his problem being due to a bad GAL, I reprogrammed the GALs with my "new" old Advin programmer ($100 used from eBay) and it cleared up the issues. Highly recommended, by the way, if you can get one reasonably priced. I still have the TL866 if I need it, but the Advin just seems to work without issue.

I still have to test out the IDE port (will look into making image tonight), but the leds are progressing through the proper sequence and I am able to enter monitor commands. I am ordering another oscillator to test it at 8MHz, just to see if it will work. BTW, I bought my 6120 from UTSource and the 6402 from Jameco. Both appear to be fine.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by w9gb on Wed, 08 Jun 2016 12:33:54 GMT
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Andrew -
Beautiful layout. Feedback from initial prototype testers?

Greg

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 11 Jun 2016 17:50:15 GMT
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All of the credit for the overall layout goes to Bob Armstrong @ Spare Time Gizmos for creating the design and making it available for others to use. I've re-captured the schematic into KiCAD and made a few tweaks (and some mistakes on the prototype boards!) but I can't take credit beyond that.

Attached are schematics and board plot files for V1.00. Please take a good look over the next day or two everyone - especially at the ROM address pins!. My plan forward is the following:
-Update the wiki page w/final information on V1.00, with a sub-page documenting the 0.99 board ECNs in case anyone forgets later on
-Do a small run (~5 is the lowest number that makes sense costwise) of 1.00 boards with EasyEDA and build one up on my side to confirm the tweaks we made are working, the fixed ROM data line order, offboard reset switch, PTCC for feeding power to IDE->CF adapters, etc.
-Take names for a larger batch here, on the VCF forum, and on the STG Yahoo group
-Do a larger run with PCBCart - since they save the tooling it makes future repeat orders less expensive.

I have also been mulling over offering sets of HD-6120/HD-6402 or HD-6120/HD-6402/GALs/EEPROMs. This is certainly a hobby project and I don't want people to expect a ton of hand-holding in building their boards...so maybe that's not such a great idea? What do you guys think?

File Attachments
1) SBC6120-RBC-DRAFT-1.00-brd.pdf, downloaded 611 times
2) SBC6120-RBC-DRAFT-1.00-sch.pdf, downloaded 548 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Sun, 12 Jun 2016 09:01:53 GMT
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Hi Andrew,

Looking over your work, as per request, I found a few points of interest on the board:

I would assume that J2 (IDE) pin 20 - F2 -J16 pin 2 (essentially the IDE VCC input) should be in the SUPPLY net class.
I would move the extra RESET connector J17 slightly more inward, as the connections now are routed outside of the board margin.
Suggest rotating C8, C9 and C19 to locate them better to the VCC pins
Carried over from the original design: decoupling cap C12 is ineffective, as the VCC pin of U18 (52C55A) is pin 26. The cap should be located near this pin.
Maybe you should assign 'keepout' areas around the mounting holes, as several traces run the risk of being compromised by mounting hardware

I think the schematics are sound. I have been imitating your work; converting the original into kicad. Very instructional, and it makes checking a lot easier.
I would have wired the datalines of the RAM identical to the ROM (6 lines per IC and "big-endian") but there is no need to introduce cosmetic changes like this, running the risk of newly introduced errors.
Also I made library components for the HD-6120, HD-6402, 52C55A and GALs, conforming to Bob Armstrongs original layout. Additionally I used the 628128 component for the RAM. Maybe this is something you would want to use for the "release" schematics.

I attached my library in case you are interested.

RHK

File Attachments

1) SBC6120.lib, downloaded 520 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sun, 12 Jun 2016 16:19:23 GMT
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>offering sets of HD-6120/HD-6402 or HD-6120/HD-6402/GALs/EEPROMs

I found the HD-6120 the only part that was hard to source. I had issues programming the GALs (the Atmel parts I had ordered were not supported by my programmer).

I think offering the HD-6120 and programmed GALs and EEPROMs would be a good idea and would make the board accessible to many more builders.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 13 Jun 2016 04:09:16 GMT
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rhkoolstar wrote on Sun, 12 June 2016 02:01I would assume that J2 (IDE) pin 20 - F2 -J16 pin 2 (essentially the IDE VCC input) should be in the SUPPLY net class.

It should be, updated this. I'll need to re-route the board in Freerouting as a result, so let's get any final changes in now!

Quote:I would move the extra RESET connector J17 slightly more inward, as the connections now are routed outside of the board margin.

Also a good suggestion, I moved this inward and away from U21 a hair as well.

Quote:Suggest rotating C8, C9 and C19 to locate them better to the VCC pins

I rotated C9 & C19, but C8 is in the correct orientation for U11 (IOT 2 GAL) vs U21 (flip-flops for POST LEDs). U11 is more important, so I left C8 as-is.

Quote:Carried over from the original design: decoupling cap C12 is ineffective, as the VCC pin of U18 (52C55A) is pin 26. The cap should be located near this pin.

The original design was 4 layers so all the capacitors are basically working together as capacitance between the 2 inner layers (power/GND). I'll go ahead and move this over for the benefit of our new 2-layer design.

Quote:Maybe you should assign 'keepout' areas around the mounting holes, as several traces run the risk of being compromised by mounting hardware

The original board has traces routed near the holes, and the FP6120 manual specifies the use of nylon mounting hardware. I'd rather not constrain the Freerouting algorithm any more than I have to.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 13 Jun 2016 16:28:57 GMT
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After making the updates mentioned, the board re-routed down to only 41 vias (10 less than the prior run!). I think rotating the 2 caps and moving C12 made the larger SUPPLY-class traces simpler and opened up more room to route the other traces.

I'll get new .pdfs out for everyone to review late this evening, but things are looking pretty good!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by djones60 on Mon, 13 Jun 2016 17:14:31 GMT
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Sounds great. Making some real progress.

I'll also second the other comment about the 6120/GAL/EPROM's. Not everyone will need them but I can see where some would.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Mon, 13 Jun 2016 18:31:14 GMT
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Looks great.

Happy to help with burning GAL's and EPROM's for folks as needed.
Thankfully the 6120's are easy to source now thru Ebay or UTSource.

Only a minor suggestion to very clearly mark U11 as in reversed orientation. It's easy to forget and destroy a GAL (from experience)...

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 16 Jun 2016 05:32:12 GMT
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Updated file are attached, based on rhkoolstar's feedback.

Take a final look over the next day or two, and then I'll be ordering handful of these from EasyEDA.

Still planning to do the larger batch with PCBCart to get nicer boards in the end.

File Attachments
1) SBC6120-RBC-DRAFT2-1.00-sch.pdf, downloaded 507 times
2) SBC6120-RBC-DRAFT2-1.00-brd.pdf, downloaded 535 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Thu, 16 Jun 2016 07:10:17 GMT
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Hi Andrew,

Looking good I'd say.

One last (cosmetic) remark: Note 1 on the top level sheet is no longer valid . Sorry for not noticing

this before...

I would like to be considered for one of the boards if possible. I have all of the parts available, including programmed GALs and EPROMs.
Testing should not take long.

RHK

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 18 Jun 2016 18:32:06 GMT
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Okay, since there are no other comments I'm going to fix Note 1 on the schematic and remove the 'Draft' designation and call this v1.00.

I'll order 5 v1.00 boards from EasyEDA. These will be green solder mask / HASL finish / 2 oz cooper. I need 1 to build up and test here, rhkoolstar gets 1 so we can add a new person testing v1.00 & the 'mini front panel' can get tested, and there will be 3 left. If anyone else is interested in building up 1 of those three v1.00s, let me know. I am 99% sure the layout is correct now, but we might still find some small tweaks are needed.

Once I can test a v1.00 board, I'll do posts in the Yahoo group, VCF DEC forum, etc to collect names for a larger run from PCBCart. I am leaning toward offering the HD-6120/HD-6402/EEPROM/GAL kits as well - probably as a 1-time run for now due to the time involved in programming/testing. I plan to add ZIF sockets stacked on top of my board so I can test the chips as a set before sending them out.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by w9gb on Sat, 18 Jun 2016 19:06:14 GMT
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Andrew,
Great. I will hold-off on acquiring the HD-6120 ... since you will be sourcing those 4 parts.

greg

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Sat, 18 Jun 2016 20:41:29 GMT
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I'm pretty sure you've got it right. I've been putting Bob Armstrong's schematics into Kicad too (without "peeking"), and I could not spot any meaningful differences between your and my

renditions. It is a great way to find out how things work.

After I validate my GALs and EPROMS I'll be happy to partake in providing programming services. It would be great if we could have "localized services" to keep the cost of postage to a minimum.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Sat, 18 Jun 2016 21:20:45 GMT
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If there are spares I'd be happy to put together one of the V1.0 boards. I have all of the parts here already.

Also happy to help with distributing GAL's and EPROM's.

Should we look into making an image of the OS-8 Compact Flash disk available? I can't recall where I cobbled mine together from.
Running Adventure on vintage hardware is one of the best features of bringing this all together!

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Sat, 18 Jun 2016 21:45:17 GMT
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I believe they are on the Spare Time Gizmos website?
http://www.sparetimegizmos.com/Hardware/SBC6120_Builders.htm , under RESOURCES

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Sat, 18 Jun 2016 21:52:10 GMT
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Might be the same images, but in case it helps, I got my OS-8 image from GRC at https://www.grc.com/pdp-8/os8utils-sbc.htm.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 18 Jun 2016 22:22:43 GMT
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I am going to dump an image of both the OS/8 OS and GAMES disks that Win32DiskImager can write directly to a CF card, to make it easier for people to get going.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 19 Jun 2016 04:20:51 GMT
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The OS/8 and Games files that are linked on the STG page and the ones at the GRC page have identical file sizes/creation dates back in 2002, so I believe they are the same files.

I've attached a 'combined image' that can be written all at once to a CF card using Win32DiskImager or dd. This was pretty easy to make, just concatenate the two .ide files into one file.

I did try to put the Adventure files on the system disk using FLX8, but it doesn't seem to run. Once I get that worked out I will post an updated image.

File Attachments
1) sbc6120_os8_games_18jun2016.img, downloaded 412 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by rhkoolstar on Tue, 21 Jun 2016 15:00:14 GMT
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Andrew,

Could I bother you for the location of the mounting holes, expansion connector and the CPREQ jumper on the board? They can be extracted from the .kicad.pcb file.

With these, I can verify the physical layout of the front panel logic and order prototypes without having to wait for the CPU board to arrive.

RHK

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 05 Jul 2016 03:07:09 GMT
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Sorry it took me so long to get back to you - attached is an updated board layout .pdf with additional dimensions added to the 'Dwgs.User' sheet to show the mounting hole and CPREQ locations.

Let me know if you need anything else.

File Attachments
1) SBC6120-RBC-1.00-brd.pdf, downloaded 449 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 11 Jul 2016 03:06:19 GMT
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Rev 1.00 test batch boards will be here Tuesday! Thanks everyone for all the feedback on this one, I'll post some pictures when I get them.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 20 Jul 2016 14:47:14 GMT
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Any update on the Rev 1.00 boards?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 20 Jul 2016 19:37:38 GMT
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The five small-run boards are here, one is sitting on my desk partly built.

Once I can check it out a bit, I will be collecting names for the larger run.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 02 Aug 2016 20:01:33 GMT
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Things are finally wrapping up with my house sale so I should get the V1.0 board finished up this week.

I didn't get a table at VCF West but I'll probably bring it with me just in case.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 04 Sep 2016 05:19:49 GMT
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Finished building the 1.00 board tonight and it booted up with the stock, non-scrambled v320 ROM files on the first try!

I need to finish testing the new features we added:
-External reset switch header

-Powering IDE->CF Adapter on Pin 20 (I plan to measure current used so I can recommend an appropriate picofuse)
-28C256 EEPROM/27C256 EPROM J15 config - EEPROM works for sure, need to test the v271 EPROMS out of my STG board to confirm that works as well.
-Try John's troublesome '373 chips to make sure the new routing improved stability of the board.

Should get that wrapped up tomorrow.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Wayne W on Sun, 04 Sep 2016 05:37:57 GMT
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Nice. Congrats Andrew.

-Wayne

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sun, 04 Sep 2016 07:48:16 GMT
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Andrew -- great work!

For the IDE power polyfuse I recommend a 500mA PPTC (see table 7 of http://rumkin.com/reference/aquapad/media/cfspc3_0.pdf)

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Sun, 04 Sep 2016 16:10:21 GMT
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Fantastic!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 04 Sep 2016 17:18:12 GMT
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The main fuse for the entire board is a 0.5A fuse, so in my mind the CF card picofuse should be something less than that.

The CF card power consumption is largely going to depend on how fast data is being transferred, and we are only using PIO mode to access the so I doubt that the power consumption will exceed the original Power Level 0 values by much.

This Transcend datasheet has some power numbers for their card - http://docs-europe.electrocomponents.com/webdocs/1111/090076 6b8111177c.pdf - max at 5V is 173mA for write and 152mA for read, in UDMA4 mode.

Sandisk has some numbers at -https://media.digikey.com/pdf/Data%20Sheets/M-Systems%20Inc%20PDFs/SanDisk%20CompactFlash%20Memory.pdf - max average 100mA at 5V

I think something like 250mA would be a good CF card picofuse setting.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 06 Sep 2016 02:57:21 GMT
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Completed testing of the following items:
-External reset switch header - works OK
-Powering Syba SD-CF-IDE-DI via power on Pin 20 - works OK
-28C256 EEPROM / 27C256 EPROM switching with J15 - works OK (tested with EEPROMs from original STG board & new EPROMs)
-The 74ACT373 chips that would not boot in the 0.99 board (unless the board was place on a non-conductive sheet on top of a metal foil sheet) - boot OK with the v1.00 board routing!

I stress tested the board with both 74HC373s and the formerly problematic 74ACT373s by running a small BASIC program to calculate the Fibonacci Sequence all the way to the largest number handled by the OS/8 BASIC. No problems.

I think I am going to make one change to the silkscreen on the final v1.00 production boards to add a note about J16 / F2 being optional.

Otherwise this is looking good. I'll work on updating the wiki page with more information this week & by next weekend hope to be collecting names for a big run of boards.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by martin8bity on Wed, 07 Sep 2016 22:19:18 GMT
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Great work! Congratulations!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 08 Sep 2016 16:03:22 GMT
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The credit really goes to Robert Armstrong for creating and making available the design & everyone who helped me test the 0.99 boards. All I really did was turn the crank on KiCAD on this one.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Mon, 26 Sep 2016 16:03:19 GMT
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Attached is a fun new image file for writing to a CF card using Win32DiskImager or dd. With the latest (2014) updated version of OS/8 Adventure!

It has two drives - SYS:/DSK: (same drive) is the OS/8 / source code / compiled binary image from Rick Murphey's Adventure site and IDA1: is the BASIC games image from the original Spare Time Gizmos site.

To run Adventure:
.R FRTS <enter>
*ADVENT <enter>
*<ESC>
<Wait approximately 1 minute, 15 seconds for game to load>

To list the BASIC games on IDA1:
.DIR IDA1:

To run the BASIC games on IDA1:
.COMPILE IDA1:<FILENAME> <ENTER>
<Wait for game to load>

For a list of all the BASIC games, see the 2nd directory listing on
https://www.grc.com/pdp-8/os8-sbc.htm

Also on SYS: on this version of OS/8 is a version of the TECO editor that uses VT100 escape codes to move the cursor around the screen, etc - I haven't played with that too much but it seems like it could be pretty useful.

(This is a somewhat later version of OS/8 'V3T' than the one in the other SBC6120 images 'V3Q', for some reason running BASIC directly does not seem to work properly but using COMPILE does even though it doesn't actually compile anything - if anyone can figure this out it would be greatly appreciated. The version of FORTRAN IV on the original SBC6120 OS/8 image was missing PASS2O.SV and could not compile Adventure, which took some trial and error to get running, so I created the new image instead using a version I knew would work.)

File Attachments

1) sbc6120-os8-advent-plus-basic-games_25sept2016.img, downloaded 370 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 15 Oct 2016 20:26:35 GMT
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I noticed something strange in my testing. Out of 3 different brands/types of CF cards that I

tested, 1 card hangs on bootup:

-Random Canon 32MB card that was a pack-in with a digital camera in 2005 - OK
-Kingston 4GB card 'CF/4GB' - OK
-SanDisk Ultra 4GB 25MB/s - HANGS

The first thing I tried was soldering a 22uF capacitor to the bottom of the board between J2-Pin 20 (CF card power) and GND, thinking maybe the CF card needed some additional decoupling. But that didn't seem to help.

The next thing I checked was the voltage making it to the CF card - only 4.73V! Then I checked directly on the output of the main board fuse (F1) and found that that voltage was only 4.73V. There was over 300mA of voltage drop across F1. Interesting.

So I made some measurements of the STG SBC6120 and the SBC6120-RBC Edition Rev 1.00 (without the CF card drawing power):
-STG SBC6120 - current draw ~103 mA, F1 resistance 1.3 ohm, voltage drop across F1 = .133 V, voltage at IC Vccs = 5.04 V
-SBC6120-RBC Edition 1.00 - current draw ~207 mA, F1 resistance 1.5 ohm, voltage drop across F1 = .310 V, voltage at IC Vccs & CF card = 4.83 (!) V

Hm, interesting, the RBC Edition is drawing 2x the current of the original STG board. I wonder why?

I narrowed the issue down to the GALs. My new Rev 1.00 board was using Lattice GALs, while the original STG chips are the lowest-power version of the Atmel ATF chips. A final measurement with switched chips confirmed this:
-SBC6120-RBC Edition 1.00 w/STG Atmel GALs - current draw 105 mA, F1 resistance 1.5 ohm, voltage drop accross F1 = .157 V, voltage at IC Vccs & CF card = 4.97 V - SanDisk CF card boots OK!

There's a couple potential solution here for people wanting to power their cards on Pin 20:
-Use the lower-power Atmel ATF GALs (ATF16V8BQL-15PU & ATF22V10CQZ-20PU) to keep the overall board current draw and hence the voltage drop across F1 lower
-Install a fuse with a lower nominal resistance, for example a .750 A fast-blow fuse (http://www.littelfuse.com/~/media/electronics/datasheets/fuses/littelfuse_fuse_251_253_datasheet.pdf.pdf) has a nominal resistance of only .175 ohms.

On further consideration though - I do think additional decoupling of the CF card is prudent & I have gone ahead and added a location for another 47 uF capacitor just *after* the fuse, just before J2-Pin 20.

That rolls the Rev to 1.10, it should the last change before we go to mass production!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by sparetimegizmos on Sat, 15 Oct 2016 22:32:03 GMT

Quote:the RBC Edition is drawing 2x the current of the original STG board. I wonder why?

More GALs. As you figured out, the 22V10 chips are fairly power hungry...

Bob

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sat, 23 Dec 2017 15:38:16 GMT

Hey

Just got out my SBC6120 today to write some software.

Can't seem to get it to run even simple BASIC programs. I'm using the "sbc6120_firstrun_25sept2016.img" disk image from the RBC wiki. Tried a couple of CF cards with the same results.

I know on this first PCB rev some of the decoupling caps are not correctly connected so I've added extra decoupling on the rear of the board between VCC/VSS on the CPU, RAMs, UART, 8255, and all three GALs. No change.

Here's a log of what I see:

```
(hardware reset)
SBC6120 ROM Monitor V271 Checksum 3732 7215 6243  15-APR-04 10:28:05
Copyright (C) 1983-2004 Spare Time Gizmos.  All rights reserved.

NVR: 0KB - Battery FAIL
IDE: 2001MB - SILICONSYSTEMS INC 2GB

>B
-IDA0

.R BASIC
NEW OR OLD--NEW
FILE NAME--FOO

READY
10 PRINT "HELLO WORLD"
20 GOTO 10
RUN

FOO     BA    7A
```

?Halted at 17403
PC>7403 PS>1011 AC>0000 MQ>0000 SP1>0000 SP2>0000

>
(hardware reset)
SBC6120 ROM Monitor V271 Checksum 3732 7215 6243 15-APR-04 10:28:05
Copyright (C) 1983-2004 Spare Time Gizmos. All rights reserved.

NVR: 0KB - Battery FAIL
IDE: 2001MB - SILICONSYSTEMS INC 2GB

>B
-IDA0

.BASIC
NEW OR OLD--NEW
FILE NAME--FOO

READY
10 PRINT "HELLO WORLD"
20 GOTO 10
RUN

FOO   BA   7A

?Panel trap at 67777
PC>7777 PS>1066 AC>1035 MQ>0000 SP1>0000 SP2>7777

>

Note the only different between the two sessions above is how BASIC is invoked - "R BASIC" versus just "BASIC". Not entirely sure what the difference is. Each fails in its own way, consistently.

Any suggestions for what is wrong or what I might try?

PS behaviour is identical with CPU clocked at 5MHz and 8MHz, and with two different power supplies (rated 3A and 2.5A; board draws only 0.2A)

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 23 Dec 2017 16:05:47 GMT
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Will - it's much more likely that this is a problem with my image file than with you hardware.

I'm honestly not much of an OS-8 expert and my focus with that image was fixing some FORTRAN issues so I could compile/run the latest version of PDP-8 Adventure on it.

I thought I had tested some of the BASIC games and they ran fine though.

I'll burn a fresh image and try the same set of commands and see what I get back.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sat, 23 Dec 2017 16:34:12 GMT
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Ah, clever chap.

Switched to using "SBC6120.ide" downloaded from grc.com and BASIC is working (once I'd figured out what "ME 10" meant!)

```
LIST

FOO     BA    5B

10 FOR A=1 TO 5
20 PRINT "NUMBER"; A
30 NEXT A
40 END

READY
RUN

FOO     BA    5B

NUMBER 1
NUMBER 2
NUMBER 3
NUMBER 4
NUMBER 5

READY
```

Much better!

Subject: Re: New Board Development - SBC6120-RBC Edition

Posted by Andrew B on Sat, 23 Dec 2017 16:45:32 GMT
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I'm glad the problem was on my end.

I'll see about fixing my image file.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sat, 23 Dec 2017 17:27:43 GMT
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Hehehe. Haven't written a BASIC program for years!

```
LIST

GUESS   BA    5B

10 LET N=1
20 LET X=10000
30 LET C=0
35 PRINT "CHOOSE A NUMBER FROM";N;"TO";X;"AND I WILL TRY TO GUESS IT."
40 IF N=X THEN 300
42 LET G=INT(N+(X-N)/2)
44 LET C=C+1
50 PRINT "IS YOUR NUMBER BIGGER THAN";G;"(Y/N)";
60 INPUT A$
70 IF A$="Y" THEN 100
80 IF A$="N" THEN 200
90 GOTO 50
100 LET N=1+G
110 GOTO 40
200 LET X=G
210 GOTO 40
300 PRINT "YOUR NUMBER IS"; N
310 PRINT "IT TOOK ME";C;"QUESTIONS."
320 END

READY
RUN

GUESS   BA    5B

CHOOSE A NUMBER FROM 1 TO 10000 AND I WILL TRY TO GUESS IT.
IS YOUR NUMBER BIGGER THAN 5000 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 2500 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 1250 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 625 (Y/N)?N
```

IS YOUR NUMBER BIGGER THAN 313 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 157 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 79 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 40 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 20 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 10 (Y/N)?Y
IS YOUR NUMBER BIGGER THAN 15 (Y/N)?N
IS YOUR NUMBER BIGGER THAN 13 (Y/N)?Y
IS YOUR NUMBER BIGGER THAN 14 (Y/N)?N
YOUR NUMBER IS 14
IT TOOK ME 13 QUESTIONS.

READY

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Tue, 26 Dec 2017 18:58:02 GMT
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Just in case this proves useful to anyone:

I got rather tired of lugging a USB RS232 adapter, RS232 null modem cable, and a 5V power supply around in order to use my SBC6120. I've been mainly working with it on my laptop in various places around the house, but our house has a real dearth of power sockets (several times I've ended up running a mains extension lead halfway across the room).

I measured the power consumption of my SBC6120, including IDE to CF adapter and CF card, as about 200mA. USB can easily deliver this. I decided to implement a simple mod to give the board a USB interface to deliver both power and data. I'm using an FTDI232RL breakout board (search ebay for "mini FTDI232"; it's the same part John's 4UART ECB board uses).

I removed the MAX232CPE chip (U17) leaving an empty socket. I then stacked a second 16-pin dual-wipe socket on top of this socket, and soldered short wires into the sockets for pins 10, 12, 15 and 16. I then connected those to RX, TX, GND and VCC (respectively) on the FTDI board. Finally I glued the FTDI board on top of the molex power socket with a bit of hot snot.

Only been using it for a short while, but it seems to work well. I now have just a single USB lead running to my laptop. The mod is easily reversible, just pop out the stacked socket and replace the MAX232 to restore the original functionality.

One minor caveat: This mod bypasses the 500mA fuse at F1.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Tue, 26 Dec 2017 19:56:21 GMT
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Photo attached.

File Attachments

1) sbc6120-usb.jpg, downloaded 1782 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by djones60 on Wed, 27 Dec 2017 06:13:29 GMT
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Very cool. I may have to give that mod a try. It sure is a cleaner set up.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Wed, 27 Dec 2017 23:35:00 GMT
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I am working on producing new disk images for OS/8 on SBC-6120 (mainly as an excuse to learn more about this machine).

The easiest way to create a bootable OS/8 image seems to be to run OS/8 itself inside a simulator and get it to build the disk image itself. However the SIMH simulator does not support the IDE interface that SBC-6120 uses, so we can't attach the disk, the OS/8 ID01 handler cannot run, and so we can't create a bootable disk image. There's another simulator (WinEight) which does support everything required, I believe this is what was used to create the current disk images, however WinEight is not easily scriptable and it's win32 software. Note that WinEight will run under Linux using wine (Yo dawg I heard you like simulation, so I put an simulator in your simulator so you can simulate while you simulate...)

I have therefore extended SIMH to support the ID01 disks and the BTS6120 "panel request" IOTs used for IDE disk transfers. The attached patch implements this functionality. It is only very lightly tested but it works well enough to boot up OS/8 from the SBC6120 disk images, so we're on the right path at least. It could be easily extended to implement other functionality eg the VM01 SRAM disk, etc.

Next I'm going to work on doing an installation by hand to learn what needs to be done to build the ID01 handler and integrate it with OS/8, and then getting the PiDP/8 "mkos8" script to work so that we can benefit from the work being done on that project to build OS/8 disk images from the distribution tapes.

In the course of writing this I discovered that the BTS6120 source code is really quite excellently documented. Hats off. I would have given up long ago without that documentation.

File Attachments

1) simh-bts6120.patch, downloaded 514 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Thu, 28 Dec 2017 23:40:51 GMT
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I've prepared updated disk images based on the PiDP/8I project. These have a good selection of software including ADVENT (to run it - "R FRTS <enter> ADVENT <escape>", be warned it takes a minute or two while it starts up). They also include the full source code for the OS and utilities. Note that the OS/8 image includes the ID01 handler (for IDE disks) but not the VM01 hander (for SRAM disk).

I suggest you write all four images to the IDE disk (in linux do "cat *.img | sudo dd bs=1M of=<device>"). This will give you four drives in OS/8 named SYS:, IDA1:, IDA2: and IDA3:.

I had a minor problem working with the PiDP/8 disks -- in particular the DIR command outputs a form-feed character (ASCII 12) after completing its work. This is a pain on a video terminal as it erases the screen!

I assembled DIRECT.PA, examined the listing and figured out which two instructions to convert to NOPs to stop this behaviour. The patched version is on these disks.

There's also a C compiler on here, not tried it yet.

Disk images are attached to this post.

File Attachments
1) 2017-12-28-disk-images.zip, downloaded 450 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Fri, 29 Dec 2017 14:10:39 GMT
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Instructions in case anyone wants to produce their own disk images from the PiDP8 distribution;

```
# start with pidp8i-v20171222.zip
# apply my SIMH BTS6120 patch; note that patching the makefile will fail,
# instead hand patch Makefile.in so it includes pdp8_bts.o in the simh executable
./configure --os8-vtedit
make
cd bin
# we need a couple of files from the BTS6120 source code;
# copy ID01.PA here, make a copy named ID01NS.PA
# copy VM01.PA here, make a copy named VM01NS.PA
# edit ID01.PA, enable SYS=1 line
# edit VM01NS.PA, comment out SYS=1 line
ls *.PA > sbc6120.list
```

```
./txt2os8 --tu56 sbc6120
dd if=/dev/zero bs=2M count=1 of=id0.disk1
cp id0.disk id1.disk
cp id0.disk id2.disk
cp id0.disk id3.disk
./pidp8i-sim
attach id0 id0.disk
attach id1 id1.disk
attach id2 id2.disk
attach id3 id3.disk
attach rk0 os8v3d-patched.rk05
attach rk1 os8v3d-src.rk05
attach dt0 sbc6120.tu56
boot rk0
ASSIGN SYS DSK
R FOTP
SYS:<DTA0:/L
^C
PAL ID01
PAL ID01NS
PAL VM01
PAL VM01NS
RUN SYS BUILD
UN RK8E
UN PT8E
UN TC
UN TC08
UN RX01
UN LPSV
IN RK05:RKA0,RKB0
DE RKA2
DE RKB2
LO VM01NS
LO ID01
IN ID01:SYS,IDA1-5
IN VM01:VMA0-1
DSK=ID01:IDA1
BO
Y
RUN RKA0 FOTP
SYS:<RKA0:/L
^C
R CCL
GET SYS PIP
ODT
13643/      5300 ^J
13644/      1    ^J
^C
```

```
SAVE SYS PIP
GET SYS DIRECT
14064/      7000 ^J
14065/      7000 ^J
^C
SAVE SYS DIRECT
ZERO IDA1:
ZERO IDA2:
ZERO IDA3:
RUN SYS FOTP
IDA1:<RKB0:/L
IDA2:<RKA1:/L
IDA3:<RKB1:/L
^C
SQUISH IDA1:
Y
SQUISH IDA2:
Y
SQUISH IDA3:
Y
SQUISH SYS:
Y
RUN SYS BUILD
UN RK8E
UN PT8E
UN TC
UN TC08
UN RX01
UN LPSV
UN RK05
LO SYS:VM01NS
LO SYS:ID01
IN ID01:SYS,IDA1-7
IN VM01:VMA0-3
DSK=ID01:IDA1
BO
# at this point we're done; quit SIMH (Ctrl-E; quit) and copy the id?.disk images to your SBC6120
```

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Mon, 01 Jan 2018 20:43:36 GMT
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My first PDP-8 assembler program. Designed to solve Project Euler problem 2: "By considering the terms in the Fibonacci sequence whose values do not exceed four million, find the sum of the even-valued terms."

The obvious difficulty here is that 4,000,000 is a lot more than 4,096 so I had to learn how to use multiple precision arithmetic. The other difficulty is converting multiple precision numbers to decimal -- I decided to punt that one to another day and work entirely in octal instead.

```
 *200
START, CLL CLA   / CLEAR LINK, ACCUMULATOR
 TLS   / OUTPUT NUL TO TERMINAL
NEXTFIB,JMS CALCFIB  / CALC NEXT FIB SEQ NO
 TAD (DWB)  / PRINT NEXT FIB NO
 JMS PRINTD
 JMS CRLF
 JMS CHKDONE  / COMPARE DWB TO TARGET
 SZL   / CHKDONE RETURNS LINK SET IF OVER TARGET
 JMP RESULT  / PRINT RESULT AND QUIT
 / TEST IF FIB NO IN DWB IS EVEN
 CLA IAC   / AC = 1
 AND DWB+1  / AC = LSB OF DWB
 SZA   / SKIP NEXT IF EVEN
 JMP NEXTFIB  / IT'S ODD - NEXT FIB
 / UPDATE SUM: CALCULATE SUM=SUM+DWB
 CLL CLA
 TAD SUM+1
 TAD DWB+1
 DCA SUM+1
 RAL   / CARRY
 TAD SUM
 TAD DWB
 DCA SUM   / SUM UPDATED
 JMP NEXTFIB

TARG, 1720   / TARGET: 4,000,000 (DEC)
 4400
DWA, 0
 1
DWB, 0   / FIB SEQ NO STORED HERE
 0
SUM, 0
 0
DWT, 0
 0

/ PRINT RESULT AND TERMINATE CLEANLY
RESULT, JMS CRLF
 CLL CLA
 TAD (SUM)
 JMS PRINTD
 JMS CRLF
```

```
 JMP 7600  / RETURN TO OS/8 MONITOR

/ CHECK IF DWB > TARG
CHKDONE,0
 CLL CLA
 / COMPUTE DWT=TARG-DWB
 TAD DWB+1
 CLL CMA CML IAC  / FORM 13-BIT NEGATIVE (NO PREV BORROW)
 TAD TARG+1
 DCA DWT+1
 RAL   / PROPAGATE COMPLEMENTED BORROW
 TAD DWB
 CMA CML IAC  / FORM 13-BIT NEGATIVE (WITH PREV BORROW)
 TAD TARG
 DCA DWT
 / LINK IS NOW SET IF RESULT WAS NEGATIVE
 JMP I CHKDONE

/ CALCULATE NEXT NUMBER IN FIB SEQUENCE
CALCFIB,0   / RETURN ADDRESS
 CLL CLA
 / COMPUTE DWT=DWA+DWB
 TAD DWA+1
 TAD DWB+1
 DCA DWT+1
 RAL
 TAD DWA
 TAD DWB
 DCA DWT
 CLL CLA
 / DWA=DWB
 TAD DWB+1
 DCA DWA+1
 TAD DWB
 DCA DWA
 / DWB=DWT
 TAD DWT+1
 DCA DWB+1
 TAD DWT
 DCA DWB
 / NEXT FIB SEQUENCE NO IS NOW IN DWB
 JMP I CALCFIB

 PAGE

/ PRINT CR+LF (NEWLINE)
CRLF, 0
 CLL CLA
```

```
 TAD (215)
 TSF
 JMP .-1
 TLS
 CLL CLA
 TAD (212)
 TSF
 JMP .-1
 TLS
 JMP I CRLF

/ PRINTD - PRINT A DOUBLE WORD AS 8 OCTAL DIGITS
/ ENTER WITH ADDRESS OF DOUBLE WORD IN AC
PRINTD, 0   / RETURN ADDRESS
 DCA DWADDR  / SAVE ADDRESS OF DWORD
 TAD I DWADDR  / LOAD FIRST WORD
 JMS PRINTO  / PRINT 4 DIGITS
 ISZ DWADDR  / INCR ADDRESS
 CLL CLA   / CLEAR ACCUMULATOR AND LINK
 TAD I DWADDR  / LOAD SECOND WORD
 JMS PRINTO  / PRINT 4 DIGITS
 JMP I PRINTD  / RETURN
DWADDR, 0   / STORAGE OF DWORD ADDR

/ PRINTO - PRINT A WORD (IN AC) AS 4 OCTAL DIGITS
PRINTO, 0   / RETURN ADDRESS
 DCA WORD
 TAD (-4)  / NUM ITERATIONS
 DCA DIGITS  / SAVE DIGIT COUNT
PRINT1, CLL CLA   / CLEAN UP
 TAD WORD  / GET REMAINING BITS
 CLL RTL   / SHIFT LEFT 2 BITS
 RTL   / THEN 2 MORE (REMEMBER LINK)
 DCA SAVCHR
 TAD SAVCHR
 RAR   / RECOVER LINK BIT
 DCA WORD  / REMEMBER IT
 TAD SAVCHR  / GET DIGIT BACK
 AND (7)   / JUST 1 DIGIT PLZ
 TAD ("0)  / CONVERT TO ASCII
 TSF   / CHECK TERM READY
 JMP .-1   / LOOP IF NOT
 TLS   / OUTPUT CHAR TO TERM
 / GET READY FOR NEXT DIGIT
 ISZ DIGITS  / ENOUGH YET?
 JMP PRINT1  / NO; DO ANOTHER!
 JMP I PRINTO  / YES; RETURN
```

DIGITS, 0
SAVCHR, 0
WORD, 0

Here's the output from running the program:

.PAL PE2
ERRORS DETECTED: 0
LINKS GENERATED: 6

.LOAD PE2

.START
00000001
00000001
00000002
00000003
00000005
00000010
00000015
00000025
00000042
00000067
00000131
00000220
00000351
00000571
00001142
00001733
00003075
00005030
00010125
00015155
00025302
00042457
00067761
00132440
00222421
00355061
00577502
01154563
01754265
03131050
05105335
10236405
15343742
25602347

21463144

.

21463144 octal = 4613732 decimal. I believe this is the correct answer!

Took less than 5 minutes to solve this problem in Python on a modern machine. Took the better part of a day to write this on the SBC6120; a lot of that time was spent learning to apply the machine's instruction set, battling with EDIT.SV (not the worst editor I've ever used, but close), and debugging with ODT (which sorely lacks a "single step" command -- unless I've missed it?)

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by b1ackmai1er on Wed, 03 Jan 2018 09:01:13 GMT
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Nice work ... it made me think of this quote ...

"We choose to go to the Moon! ... We choose to go to the Moon in this decade and do the other things, not because they are easy, but because they are hard; because that goal will serve to organize and measure the best of our energies and skills, because that challenge is one that we are willing to accept, one we are unwilling to postpone, and one we intend to win ..." (JFK / wikipedia)

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by trick-1 on Tue, 17 Jul 2018 00:57:17 GMT
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Hi Folks

Another SBC6120 lives!
Finally got around to building the board in December 2017. Only just had a chance to build the serial cable (yes I know) power it up and test. Happy to say worked first go

Attached are some photos....now to find a suitable case...

Thanks for a great board.

Cheers

Richard

File Attachments

1) IMG_8321.JPG, downloaded 473 times

2) IMG_8322.JPG, downloaded 458 times

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by djones60 on Tue, 17 Jul 2018 01:12:48 GMT
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Congrats!! I know how it goes. I have a major back log of things to build. I figure one of these days I'll retire and have time for it all

David

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by frax on Tue, 17 Jul 2018 08:12:24 GMT
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I would love to buy one If anyone got an extra kit?!? Ok, my backlog is kinda full to but PDP always get priority

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by djones60 on Wed, 15 Aug 2018 15:13:41 GMT
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I can't remember if anyone has asked this before or not. But has anyone interfaced the SBC6120-RBC with the PiDP case and switches? I was thinking that would be a really cool case for this board.

David

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 15 Aug 2018 16:48:29 GMT
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The front panel was a later add-on to the SBC6120 - the board was initially designed to be used completely with the monitor ROM.

The updates to the PDP 8/e style front panel LEDs selected by the rotary switch are driven by at timed interrupt in the monitor code which reads the switch position and updates the LEDs based on which item is selected.

The PDP 8/i style front panel doesn't have the rotary switch and has more LEDs so everything can

be shown at once.

To interface with the PiDP 9/i style front panel would require not only custom interface hardware but also updates to the ROM monitor to update all of the LEDs on every tick of the front panel update interrupt, instead of just the values selected by the rotary switch.

Certainly someone could try to do this, but it would be a bit of work.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by boss on Sat, 18 Aug 2018 23:48:30 GMT
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Hi Andrew,
I spent most of my life with DEC company. Started in sixties with PDP-11, continued with VAX 32 bit till latest 64 bit Alpha computers. But never ever has had an opportunity to play with the PDP-8. Is the prototype board still for sale?
Regards
BoSS

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 19 Aug 2018 02:42:08 GMT
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I have plenty of the final V1.1 PCBs, $20/each. Shoot me an email at abingham (at) gmail.com

---

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by borutk on Tue, 04 Sep 2018 10:43:20 GMT
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Is there a way to transfer binary files from a PC to SBC6120 IDE drive via serial port?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Thu, 06 Sep 2018 21:17:43 GMT
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Kermit-12 should be able to do this, but I have not done it myself - http://www.columbia.edu/kermit/pdp8.html - I *think* one of the two disk images may include it? If not I can look at getting it added.

You can load an entire disk image over the serial port using the Monitor ROM - that should be

covered in the User's Manual - but it's quite slow to do so, much quicker to write the image from a PC with an IDE interface (hard disk) or CF card reader.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by borutk on Fri, 07 Sep 2018 07:45:25 GMT
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It would be great if something like Kermit was on one of the included images. There is a lot of old PDP8 software on the net that i would like to try,
but the method of transferring the files via SIMH to disk image and then dd-ing the whole image is way too complicated to even try and it also deletes
the existing image from the CF card, which i would like to keep.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 09 Sep 2018 01:53:58 GMT
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Quote:It would be great if something like Kermit was on one of the included images. There is a lot of old PDP8 software on the net that i would like to try, but the method of transferring the files via SIMH to disk image and then dd-ing the image is way too complicated to even try and it also deletes the existing image from the CF card, which i would like to keep.

I'll take a look at this in the next day or two - I agree having a solution to do this would be great and ideally documented on the Wiki page.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 09 Sep 2018 17:57:15 GMT
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So, both disk images that I have posted on the wiki have Kermit-12 on them. The file name is 'K12MIT.SV'.

On the newer 'sbc6120_firstrun_25sept2016.img' image it's directly on the SYS: (IDA0) drive and and be run directly via 'R K12MIT', on the original 'sbc6120_os8_games_18jun2016.img' image it's on IDA1: and can be run via the following two commands:
GET IDA1:K12MIT.SV
START

Once you run Kermit, you can using the RECEIVE command in Kermit on the SBC6120 side and then send files over via the Kermit protocol from the modern PC. I tested this in Tera Term.

Subject: Re: New Board Development - SBC6120-RBC Edition

Posted by pbirkel on Sun, 09 Sep 2018 18:19:01 GMT
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Thanks! The files listed at the bottom of:

https://www.retrobrewcomputers.org/doku.php?id=boards:sbc:sb c6120-rbc-edition:start

Are currently dated 2017-02-05. Are those dates now incorrect?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 09 Sep 2018 21:37:06 GMT
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I did not make any updates to the images, just checked to verify that Kermit was included - the dates in the filenames are the dates they were generated, the dates in the table is when I uploaded them to the wiki page.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by pbirkel on Mon, 10 Sep 2018 06:03:11 GMT
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Thank you for the clarification :-}.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by borutk on Mon, 10 Sep 2018 10:41:07 GMT
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Thanks Andrew, i'll check it out.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by borutk on Tue, 11 Sep 2018 07:38:24 GMT
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If anyone wants to stock on spare HD1-6120-9C, there is a Chinese seller selling them at $22.79 on eBay:
https://www.ebay.com/itm/1pcs-HD1-6120-9C-HD1-6120-9-C-DIP-4 0/392103001416
There is also the option to "Make offer".
I don't know if they work, but if you have a working SBC6120, it's easy to test the part.

Disclaimer: i have nothing to do with the seller, eBay or weather patterns above Antarctica

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 11 Sep 2018 15:57:30 GMT
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Nice to see the China prices coming down a bit. My large order of 75pcs from one of the China sellers in 2016 caused the prices from ALL of the China sellers to go up to ~$35-38 for a while. They clearly have a list somewhere of how well different 'pulled' chips sell that they share with each other. Smart! Someday I'm going to take a trip to Shenzhen to see for myself.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Jonas on Tue, 11 Sep 2018 16:01:28 GMT
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Yes the seller at https://www.ebay.com/itm/1pcs-HD1-6120-9C-HD1-6120-9-C-DIP-4 0/392103001416
is a trustworthy seller as far as I can tell. I have bought a lot of stuff there.

Another option is Utsource.net (not their eBay offerings). Search for D1-6120 (yes without the H). $12.64 for one or $11.04 for ten. I have bought two and yes, it is the HD-6120. If you search for HD-6120 at utsource.net you find the same item for an astronomical price.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by boss on Tue, 11 Sep 2018 20:43:06 GMT
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Mine 6120 chip arrived yesterday from the same eBay seller. The chip looked brand new and unused.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by b1ackmai1er on Wed, 12 Sep 2018 12:53:12 GMT
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Thank you, order a D1-6120 for $AUD21 from UTSOURCE

Jonas wrote on Tue, 11 September 2018 09:01Yes the seller at
https://www.ebay.com/itm/1pcs-HD1-6120-9C-HD1-6120-9-C-DIP-4 0/392103001416
is a trustworthy seller as far as I can tell. I have bought a lot of stuff there.

Another option is Utsource.net (not their eBay offerings). Search for D1-6120 (yes without the H). $12.64 for one or $11.04 for ten. I have bought two and yes, it is the HD-6120. If you search for HD-6120 at utsource.net you find the same item for an astronomical price.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by tingo on Wed, 12 Sep 2018 15:34:47 GMT
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So, what else fun can one do with a 6120 in addition to use it an a SBC6120?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Wed, 12 Sep 2018 15:36:37 GMT
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If someone wants to design an S-100 board that would be neat-o. But I have too many projects right now

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by djones60 on Wed, 12 Sep 2018 20:20:51 GMT
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Andrew B wrote on Wed, 12 September 2018 11:36If someone wants to design an S-100 board that would be neat-o. But I have too many projects right now

I wish I new enough about KiCad and stuff to do that. It would be an interesting project.

On a off-topic note. Anyone going to VCF Midwest this weekend ?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by hideehoo on Thu, 13 Sep 2018 18:18:03 GMT
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Yep, I'm heading there tomorrow. If anyone is interested I have enough parts (including the HD1-6120 chips) to completely build another two or three of these. Was going to put some complete kits together put haven't got around to it yet, can drag them along if someone wants to pick one up at VCF.

Here's the one I built for myself
http://www.vcfed.org/forum/showthread.php?54595-SBC6120-Retr
oBrew-Computers-Edition-KiCAD-Gerber-PCBs-amp-Partial-IC-Kit s&p=444739#post444739

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Sun, 23 Sep 2018 16:23:50 GMT
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Got my kit: thanks, Andrew! That gold-on-black board is very nicely made.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Thu, 27 Sep 2018 02:27:26 GMT
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Mine arrived today too. Unfortunately although it looked unused (and probably remarked) it is non-functional.

Have you tested the part you received?

- Gary

boss wrote on Tue, 11 September 2018 13:43Mine 6120 chip arrived yesterday from the same eBay seller. The chip looked brand new and unused.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by borutk on Thu, 27 Sep 2018 19:58:34 GMT
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Mine arrived today. It looks new and unused, but it is dead as a doornail.
My SBC6120 does not budge even with 4MHz clock.

Bo/

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Thu, 27 Sep 2018 21:22:35 GMT
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At least the good news is that I received a prompt refund from the seller.

I'm not sure what IC was remarked, but it wasn't a HD1-6120.

- Gary

borutk wrote on Thu, 27 September 2018 12:58Mine arrived today. It looks new and unused, but it is dead as a doornail.
My SBC6120 does not budge even with 4MHz clock. Bo/

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 29 Sep 2018 06:32:11 GMT
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That's a shame about the non-working chips.

I will take a look with one of my chips and see if there is some kind of an alive-ness check people can do. I think that if you feed it a clock, hold /RESET low for ~50 clock cycles and then let it go high, /LXMAR should immediately go low as it tries to latch the memory address registers. That would at least indicate that it is trying to load an instruction from RAM. /OUT, /MEMSEL, and /IFETCH should do some things a clock or two later as well.

Would an alive-ness test with a standard 5V Arduino Uno board be sufficient for most people?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by tor on Sat, 29 Sep 2018 19:04:22 GMT
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That would work for me.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by boss on Sat, 29 Sep 2018 21:37:11 GMT
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For me as well.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 30 Sep 2018 17:49:58 GMT
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I started a new thread on a simple Arduino checker to see if a chip is actually an HD1-6120:
https://www.retrobrewcomputers.org/forum/index.php?t=msg&amp ;th=328&start=0&

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Wed, 10 Oct 2018 21:22:29 GMT
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Picked up 2 more HD-6120's from UTSOURCE. They were listed as D1-6120-9C
https://www.utsource.net/itm/p/1887077.html

They appear old (some oxidation on pins, minor chips in ceramic) but original and both work perfectly.

$14.19 each, and they list 75653 in stock!!!

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Thu, 11 Oct 2018 21:44:03 GMT
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will wrote on Tue, 26 December 2017 13:58...
I measured the power consumption of my SBC6120, including IDE to CF adapter and CF card, as about 200mA. USB can easily deliver this.

Thanks for this. I may have to try it, as my recently-built SBC6120-RBC Edition successfully goes through POST but doesn't get to kick anything out the serial port. I suspect I may have fouled up the cabling. Or not found a terminal under Linux that can talk 7M1. 9-pin serial null-modems are much rarer beast these days than when the original SBC6120 came out.

One caveat about using FTDIs and the like is that - while USB can deliver 200 mA and beyond - they often negotiate to limit themselves to 100 mA. There's a milliamp rating (sometimes confusingly called "Max Power") in the USB parameters that shows you their current limit. SparkFun has a "Beefy" USB serial adapter that can deliver quite a bit more power, but is a lot more expensive.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by tingo on Thu, 11 Oct 2018 22:40:16 GMT
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FWIW, I found that simply doing 'screen /dev/ttyUSB0 9600' (or whatever your usb serial port is called) works. Of course, this was after I had spent some time trying to get usb-to-ttl adapters working (blush)...

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Fri, 12 Oct 2018 03:40:05 GMT
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Aha! The null modem cable I bought turned out to be straight-through. On rectifying, the console message came through. Yeah! Another successful SBC6120-RBC is built!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Sat, 13 Oct 2018 19:50:13 GMT
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... though I shouldn't be too happy as I'm yet to get the thing to boot successfully.

I typically get the monitor prompt, but (B) isn't accepted:

SBC6120 ROM Monitor V320 Checksum 3752 6072 3515 09-APR-10 21:15:39
Copyright (C) 1983-2010 by Spare Time Gizmos. All rights reserved.

NVR: Not detected
IDE: 489MB - LEXAR ATA FLASH
IOB: Not detected

>BBBBBBBBB
This is just from pressing B once.

I did get a card to boot once, but unfortunately my serial params were wrong and all I got was noise

Are there any hints for troubleshooting booting, please?

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 13 Oct 2018 19:57:23 GMT
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Seems like you might still have some kind of a serial problem?

If you boot without the flash card attached, and type 'h <enter>' at the prompt, do you get the monitor ROM help?

Can you dump RAM, 'e 0000-1000 <enter>'

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Sat, 13 Oct 2018 21:40:22 GMT
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I had a problem with keys repeating - they would just repeat until the monitor's input buffer was full. It turned out that the GAL at U11 was not programmed correctly (or it was a faulty chip). I swapped in a newly programmed replacement GAL at U11 and the issue went away.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sat, 13 Oct 2018 22:03:18 GMT
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These GALs came from one of my wait list kits, so they were tested to boot & run Adventure off a

CF card before being sent out. Not that there couldn't be a problem, but it would be the first I'd heard of with any of the kits or partial kits that I've sent out.

I have found that some of my CF cards are sensitive to the duration of the reset pulse and holding down the reset button for longer makes them come up. But I'd definitely recommend testing without the CF card first to make sure the monitor is running properly. (The monitor is pretty smart, when you ask for help for instance it only shows the IDE commands if there is an IDE drive detected!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Simmo on Sun, 14 Oct 2018 08:34:27 GMT
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Yeah, I picked up a D1-6120-9C ($AUD17) and a HD3-6402R-9 ($AUD4.50) from UT Source which look OK. Hopefully they work. Yet to get myself a PCB, which I'll get shortly from Andrew B, and test these chips. Looking forward to a PDP adventure game myself.

Andrew B, let us know through the boardinventory page what you have left available for the SBC6120-RBC.

Thanks,
Simmo

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 14 Oct 2018 22:07:26 GMT
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So - there have been a few people who have been waiting a long while for 'wait list' stuff. Apologies to the people who have patiently waited. I hate to take any $$ unless I know I can ship promptly, so it's been slow going since I made the giant bath of 65 original kits. I'm ordering some GALs + EEPROMs to get caught up along with more PCBs. I have a few tested 6120s left but based on the wait list I have, I believe that they are all likely spoken for at this point. If I get through the list and any are left, I'll post back here.

The mis-numbered D1-6120 from UTSource seems like a good option right now.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Mon, 15 Oct 2018 16:48:17 GMT
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Andrew B wrote on Sat, 13 October 2018 15:57Seems like you might still have some kind of a serial problem?

If you boot without the flash card attached, and type 'h <enter>' at the prompt, do you get the monitor ROM help?

Can you dump RAM, 'e 0000-1000 <enter>'
Can't seem to do either. Entering 'H<cr><lf>' at the prompt usually returns a <lf>. This last time I've tried it, all three POST lights lit up and it seems to have hung.

(I'd be happy to start another thread about this, as my serial issues must be tedious for other readers.

What I've tried/tested:
two different null modem cablestwo different serial adapterscontinuity between 6402 and MAX232: goodcontinuity between MAX232 and serial out: goodcapacitors on MAX232 are all goodReplacing the MAX232 with a socket and USB serial adapter resulted in all three POST bits lit and no useful functionreset button often doesn't work, even if held for a long time and no CF2IDE adapter present. Usually resets to just power LED and no POSTboth oscillators doing their job (or there would be no coherent monitor message)no obvious bent pins or shorts in the dual-wipe socketsI have been more careful with ESD precautions with this build than any other, given the dire warnings in the manualThe board was less compatible with my lead-free + no-clean flux soldering setup than I'd hoped(smallest CF I current have is 512 MB, and written using Etcher; I'm getting smallest cards I could find by mail this week)
Guess I'll have to trace every line and see if something's not connected.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Tue, 16 Oct 2018 03:02:50 GMT
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It sounds like you're getting to the end of all of the logical things to do.

Did you happen to substitute any of the 7400 series logic with a different series compared to what is in the BOM? We had strange intermittent issues with some 74ACT (I think?) chips on the Rev 0.99 board, but I went to thicker power & GND traces + 2 Oz copper on the Rev 1.xx boards and that seemed to resolve that issue, even the previously problematic chips worked fine.

Where did you source the rest of the chips for the build?

I don't mind if we stay in this thread or split it off, totally up to you.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Wed, 17 Oct 2018 12:37:54 GMT
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All my logic chips are TI SN74HC... types, bought new from Digikey using your BOM generator, like all the other chips. I did find one dry joint on the low EEPROM, but fixing that made no

difference. I may try the simple expedient of taking all the chips out and re-socketing them.

After that, I guess I'll have to test the logic chips one by one.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Sun, 21 Oct 2018 03:41:51 GMT
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Is there a way to get a nice connection table (basically a text version of the schematic, showing U1 P1 going to ___, U1 P2 going to ___, etc) from kicad? The schematics would be so much page flipping.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by Andrew B on Sun, 21 Oct 2018 03:52:51 GMT
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There should be a text file of the netlist in the .zip with the Gerber & KiCAD files. Take a look at SBC6120-RBC.net, in the bottom of the file all of the nets are listed.

If you want to post or send some pictures of the board, I'll take a look to see if there is anything amiss.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Mon, 22 Oct 2018 22:00:56 GMT
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Thanks, Andrew. I managed to generate a sorted by component netlist using kinparse - https://github.com/xesscorp/kinparse .

Photos are here:

Front - https://www.flickr.com/photos/scruss/44778961914/in/datepost ed/Back - https://www.flickr.com/photos/scruss/30563814977/in/datepost ed/
I fear I may have burnt off a couple of pads, so as long as there aren't too many I might be able to use patch wires. If not, I may have to come back to you for a new board.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Tue, 14 Apr 2020 01:51:29 GMT
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Wheee! I finally got this rebuilt and tested: thanks for sending those boards, Andrew!

I'm still getting no keyboard response at the monitor:

SBC6120 ROM Monitor V320 Checksum 3752 6072 3515 09-APR-10 21:15:39

NVR: Not detected
IDE: Not detected
IOB: Not detected

>H

But at lest the thing's not fried due to my terrible soldering last time!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by will on Tue, 14 Apr 2020 10:14:19 GMT
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Check hardware (RTS/CTS or DSR/DTR) flow control is disabled on your serial terminal (otherwise it may not transmit).

Pin 19 (DR) on the UART (U16) should go high when there is a character received and waiting for the PDP-8 to read out, and stay high until pin 18 (/DRR) on the same chip goes low.

These signals are both connected to IOT2 (U11) so check this chip is correctly programmed if the DR signal is apparently being ignored or /DRR is not being generated.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by gkaufman on Tue, 14 Apr 2020 13:06:03 GMT
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Not to suggest the most simple possiblility, but are you using 9600 baud, 7 bits, mark parity and 1 stop bit?

- Gary

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by scruss on Tue, 14 Apr 2020 23:09:54 GMT
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Thanks! Caught the problem on the first elimination: the USB-Serial null-modem combo was wired wrongly. Swapping it for the one on my Zeta2 made it happy.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by kb811 on Tue, 22 Sep 2020 21:17:44 GMT
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I have just built two RBC versions of the SBC6120 and am pleased to report that they appear to work fine at both 5 and 8 MHz (for example: booting into OS/8 and running adventure).

The only problem I had eventually turned out to be the Microchip ATF22V10C[QZ] devices and the TL866II Plus programmer I used to program them - the SBC6120 would start up, but there were various random behaviour issues and it wouldn't boot into OS/8. Initially I thought it might be my soldering, a PCB problem or a dodgy processor. But after lots of testing and making up a second one (that behaved exactly the same) I grew suspicious of the ATF22V10C[QZ]s and then found that things were fine using secondhand Latice GAL22V10Bs. Later, after investigating the ATF22V10C[QZ], I found out about the programming instructions described below; those devices also now work fine.

Using ATF22V10C[QZ] devices: "Condition" the device (probably true for any programmer; see below). Select the "UES" profile for the device in the TL866II Plus software when programming them.
References (where I found out about this):

The following link provides useful info about how to correctly program Microchip ATF22V10C[QZ] devices:
http:// forum.6502.org/viewtopic.php?f=10&t=6065&start=30#p7 5562

The conditioning instructions are described near the end of the webpage at the following link, to be used before programming new (and I would assume, "just in case", recently obtained or previously unconditioned) devices:
http://www.bhabbott.net.nz/atfblast.html

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by tingo on Wed, 23 Sep 2020 18:59:35 GMT
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Useful - thanks!

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by kb811 on Fri, 16 Oct 2020 21:40:40 GMT
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IOB6120

I have just completed building an IOB6120. RTC and battery backup are installed. Everything tested so far seems to be working fine! Things I haven't tried yet are the printer port, the on board serial ports or the digital I/O. Unknown: use of VMAx: from OS/8. I probably need to "exercise" it a

bit more.

I constructed Vince Slyngstad's revision of the original that he describes here http://so-much-stuff.com/pdp8/sbc6120/iob6120.php.
The original is described here https://www.jkearney.com/sbc6120/iob6120.htm.
Some additional information can be found here https://tinymicros.com/wiki/IOB6120.
NOTE: Checking the schematics is a must when constructing any of these.

OS/8 boots off a compact flash card in the IOB6120's CF socket (you need to map the partitions first).
There is one known problem: "the Fortran run-time system does not work with the IOB6120"; see http://www.sparetimegizmos.com/Hardware/SBC6120_Adventure.htm.

I wonder if this might be a VT52/IOB6120 "TTY" I/O implementation issue (TBC): whilst I was pondering why Adventure did not work and everything else seemed to, I noted that Adventure seems to be fine if you run the system via the serial port on the SBC6120 (whilst still running OS/8 off of the CF plugged in to the IOB6120). I might see if I can figure out the problem sometime.

Assembly

The PCBs I got back from fabrication had an issue with the silk screen (I don't know why). But everything else seemed to check out okay.

The first mistake I made was using solder paste! There are three SMD components with a very fine pitch, so solder paste and heat seemed to be the best way to go. This worked very well for all the other SMD components, but not the fine pitched ones (stencil, syringe and then just-daub-it-on methods tried). Maybe there was a problem with the solder mask, or my technique.

I gave up on the solder paste and started again with a soldering iron (and another fresh PCB). I used a tip just small enough that it would not immediately bridge multiple pins to solder the fine pitch pins one by one by hand (microscope/visual assistance required for this)! This was much easier than anticipated, although somewhat time consuming. Fingers crossed that all pins are actually soldered down (I double checked with the microscope twice). A very small number of bridges between pins did occur, but were easily taken care of with "solder wick" because I was soldering from the "outside". I also hand soldered all the other SMD components whilst I was at it, except for the crystal. I used solder paste and a hot air station for the crystal as that seemed easier/safer for its style of packaging and device type (but soldering it with an iron would probably have been okay).

The second mistake was the use of shrouded headers for the digital I/O headers (io1 and io2); this is currently preventing me from soldering in the CPREQ jumper extension.

Inter-board connection

I used a stacking header. I couldn't find one with the height and pin length that I would have preferred; so I opted to use two Adafruit headers designed for the Raspberry Pi (one 2x20, and 2x5 carefully cut from another; for extra strength glue was applied to the two ends that butt together just prior to them being soldered in to place). It would be better to have greater

separation between the boards (longer header pins) without looking for an additional "stacker" to build it up or needing a shield to prevent shorts (things are particularly close with the socketed crystals on the SBC6120). BTW, stacking them the other way would block direct access to the top of the IOB6120.

Whether, or not, a stacking header is really needed depends on decisions about a front panel .

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by thunter0512 on Wed, 17 Apr 2024 06:54:59 GMT
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I have been using the SBC6120-RBC for a few years, but recently Chris Tersteeg has created a nice FP6120 front panel clone of Bob Armstrong's original. I have now noticed that there may be a problem with the SBC6120-RBC because the following little count program does not behave as expected on the SBC6120-RBC + FP6120, but works fine on Bob Armstrong's original:

0: 7001
1: 2101
2: 5001
3: 5000

On the original when you select the AC with the rotary switch, the LEDs continuously count from 0000 to 7777 forever.
On the RBC version the LED display freezes at about 7777 and then resumes what is approximately one full count cycle later.
When while in the frozen state I hit break on the console or toggle the Halt switch, I see that the program is running fine - just the LEDs are not updating.

In an effort to narrow down the culprit I have now swapped replaced the SBC6120-RBC with Bob Armstrong's original and plugged that into Chris Tersteeg's FP6120 and it behaves correctly.

When I plug the SBC6120-RBC into Bob Armstrong's original FP6120 the data LEDs freeze as before. I also tried a second SBC6120-RBC and it too has the "freezing" behaviour.

This seems to indicate that there is some problem with the SBC6120-RBC. When the display is frozen I see that the CPREQ signal keeps pulsing at approx 30 Hz.

The ROM Monitor in both SBC6120 (original) and SBC6120-RBC is version V320.

The original SBC6120 and both SBC6120-RBC run OS/8 without a glitch. There is no noticably freezing of the LEDs with OS/8 on any of the 3 SBC6120.

I wonder what could cause this:

The SBC6120-RBC is a double layer board whereas the original is a 4 layer board. Possibly when AC wraps from 7777 to 0000 it causes some noise which disturbs something.

The PAL firmware may be subtly different.

Could some of you please try this if you have any FP6120 and a SBC6120-RBC.

Subject: Re: New Board Development - SBC6120-RBC Edition
Posted by thunter0512 on Thu, 16 May 2024 16:06:33 GMT
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The freezing problem was caused by a RCA 6402 UART. Harris and Intersil 6402 UARTs work fine and don't cause this freezing of the FP6120 display. The RCA UART was working fine as a UART, but somehow it caused the freezing when the count rolled over from 7777 to 0000.
