
Subject: A simple CP/M Z80 SBC without glue logic
Posted by [plasmo](#) on Thu, 14 Mar 2019 15:20:35 GMT
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I have had leisure time to daydream while traveling and waiting. The recent discussion about Z80 design makes me thinking of a glue-less Z80 SBC consists of Z80, RAM ROM, and KIO. The KIO can do CF interface to provide CP/M capability and discrete to bank switch ROM, RAM and RAM banks. No glue logic necessary. It should be a simple, compact SBC for people not wanting to fool with CPLD, a 4-chip solution in 50mmX100mm pc board. What to do with all the extra pc board space. Thought?
Bill

Subject: Re: A simple CP/M Z80 SBC without glue logic
Posted by [wsm](#) on Thu, 14 Mar 2019 17:50:16 GMT
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Interesting idea. This is similar to what I did when I started my Z180 MinZ design ... minimal components. I think there might be a COUPLE of additional chips required. Firstly, I like to always add a reset supervisor / voltage monitor which also allows a reset pushbutton. I admit to software development goofs that require resets :)

Serial I/O can be handled on a header for external USB or RS-232 adapters. I chose to make two variants of my board, one with a CP2015 USB bridge and one that allows either an RS-232 translator or a TTL header.

At first glance it appears the KIO CS* can be tied low since it also uses IORQ* and is the only I/O device. However, I think that may get into some issues with interrupt responses (M1* plus IORQ*) which would be both a vector read AND an I/O write.

The other question I would have is on the ROM / RAM chip selects. There is a need to differentiate both memory cycles (MREQ*) and RAM vs. ROM. I know there are some memories with dual selects (can't remember exact ones offhand) but many [most?] of the newer ones only have a single select and expect an external decoder.

Perhaps weak pull-up vs. pull-down on a KIO port can differentiate ROM vs. RAM on reset and until the KIO can be programmed. That still leaves the issue of differentiating I/O versus memory cycles.

Just my \$.02 while I wait for another cup of coffee to kick in. I'm thinking that you will require a decoder i.e. glue.

While you're toying with ideas, why not also look at the Z84C15 which has basically the same features of the Z80+KIO but integrates the CPU and also has memory selects. The downside is that it's a VQFP-100 package.

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [plasmo](#) on Thu, 14 Mar 2019 18:09:37 GMT

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My original thought was tying nMREQ to chip selects of both ROM and RAM, and use a switch to select which device's OE to enable. At powerup, ROM OE is selected, the software writes itself to itself, which copy ROM into RAM, so during the transition when both ROM & RAM OE are enabled, there won't be contention. I want to replace the physical switch with PIO output discrete without glue logic. Don't know if it is doable until I examine the datasheet in detail. I can always fall back to the physical switch.

I just assume I can tie IORQ and M1 directly to KIO, but I need to read the datasheet eventually.
;-)

Bill

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [mikemac](#) on Thu, 14 Mar 2019 23:39:23 GMT

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I think you meant a CP2105, not a CP2015. But I learned that a CP20151 is a Peltier cooler! :)

If you were considering using a Z84C15 for a "glueless" system, why would you not go whole hog and use a EZ80F91 instead?

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [wsm](#) on Fri, 15 Mar 2019 01:01:07 GMT

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Good catch on the CP2105. Sometimes my brain gets ahead of my fingers ... or perhaps the other way around.

I've played around a BIT with my EZ80F91 module and even started a schematic for a system. I agree that it's a highly integrated and very powerful core but it also has a learning and development curve that's bigger than a Z80 or Z180. Project # 733 :) FYI - There was someone on the COMP.OS.CPM newsgroup that was working on an eZ80-CP/M system.

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [etchedpixels](#) on Fri, 15 Mar 2019 12:21:33 GMT

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If I remember rightly the Z80 PIO ports are deliberately set up to power on as inputs so you don't risk damage during power up and configuration. I guess therefore you can use that to do the ROM/RAM select at boot time if you pull it the right way and still have plenty of spare PIO bits.

You could also save logic by tying the chip select of the KIO to something like A15 low. Quite a few home micros actually avoided lots of glue by using A15 / A14 / A13 / ... as selects for the I/O device and wired the low bits to the register select - taking the small software hit of doing `ld bc,#0x7ffx` out (c),a etc for the different devices.

If you are trying to be minimal you could also bitbang an SD card with some of the PIO bits and 5v/3.3v shifting (or just one of the cheap off the shelf adapters). If you pick the right PIO bits a Z80 at 7.3MHz can do about 18-19Kbyte/second so floppy like and good enough for CP/M. If you mix the Ax low trick with the PIO bits you have to unroll one of the loops 8 ways but it's still works nicely.

What to do with the spare space - I guess support bigger RAM as an option, and maybe have flash with a jtag programming header not ROM, oh and rc2014 connector ?

Possibly more important if it's meant to be a 'first build' would be some status LEDs and test points ?

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [wsm](#) on Fri, 15 Mar 2019 15:47:18 GMT

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Plasmo: Tying MREQ* to CS* of the RAM and ROM would work but the switching of OE* might require some glue. At power-on the ROM's OE* needs to be low and the RAM's high which can be done via pull-down / pull-up. After the copy, the ROM's OE* can go high from a KIO port. HOWEVER, the RAM's OE* needs to be tied to RD* or possibly NOT WR* after the switch to avoid bus contention during RAM writes i.e. simultaneous RD* and WR* from/to RAM.

etchedpixels: The KIO's CS* could be tied to a high address bit and that should work including if interrupts are enabled i.e. IORQ* active but RD* and WR* inactive. If the KIO is the only I/O device then it might be simpler to just tie CS* low and let the KIO decode IORQ*, M1*, RD* and WR*.

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [plasmo](#) on Fri, 15 Mar 2019 16:03:44 GMT

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The real reason is because I made a low-ball offer for a lot of KIO and it was accepted! So I need to build a board to check it out.

I think a cheap & simple design with clearly delineated functions not cluttered by interconnecting glue logic is a good educational hardware. An RC2014 expansion and blinky LEDs and push buttons are desirable additions.

Bill

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [plasmo](#) on Fri, 15 Mar 2019 16:11:09 GMT

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wsm wrote on Fri, 15 March 2019 09:47Plasmo: Tying MREQ* to CS* of the RAM and ROM would work but the switching of OE* might require some glue. At power-on the ROM's OE* needs to be low and the RAM's high which can be done via pull-down / pull-up. After the copy, the ROM's OE* can go high from a KIO port. HOWEVER, the RAM's OE* needs to be tied to RD* or possibly NOT WR* after the switch to avoid bus contention during RAM writes i.e. simultaneous RD* and WR* from/to RAM.

Looking up the datasheet of AS6C1008, I see the OE is "don't care" when WE is asserted for write operation, so I don't need to negate OE for write. Whew!

Bill

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [etchedpixels](#) on Fri, 15 Mar 2019 16:39:24 GMT

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wsm: agreed - the reason for wiring it to A15 is it means you can then attach other stuff to it later, otherwise you are constrained to the single KIO, whereas if you wire it to A15, fit an optional RC2014 connector and wire the IRQ line from the RC2014 to a PIO pin you get *all* of the RC2014 I/O features including being able to manage the RC2014 interrupt line in IM2 mode for free (more than most RC2014 CPU cards can do!). Come to think of it if you decided to pull the RAM and ROM chips I think you get all of RC2014 later if you wanted ?

Extra RAM looks more awkward though - the 512K RAMs seem to drop CE2.

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [wsm](#) on Fri, 15 Mar 2019 17:15:02 GMT

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Quote:Looking up the datasheet of AS6C1008, I see the OE is "don't care" when WE is asserted for write operation, so I don't need to negate OE for write. Whew!

I learn (or remember) something new every day. Although I've looked at various memory chip's decoders, I wasn't paying attention to the output tri-state disable when WE* is active.

I still think you'll have some data bus contention with the RAM unless OE* is connected to RD*. The Z80 WR* signal goes active roughly 1T after MREQ* goes active (#8 to #30) and thus the RAM will first be in read mode if OE* is tied low. However, the Z80 Dout goes active a minimum of 20ns before WR* (#29). The AS6C1008 will be WE# controlled and it's Dout will still be driven

for tWHZ (max 20ns) after WE#. Looks to me like the overlap is a minimum of about 32ns for a 12.5MHz Z80 and possibly a lot longer.

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [plasmo](#) on Sat, 16 Mar 2019 13:41:49 GMT

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Thanks for the analysis. It is close enough, I'll go ahead and layout the board but have the option of adding 8 isolation resistors in the data lines. KIO has arrived so I'm anxious to try it out.

Bill

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [plasmo](#) on Thu, 04 Apr 2019 12:34:34 GMT

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Here is the KIO test bed with zero-glue-logic Z80. I add a toggle switch to simplify the switching between ROM and RAM: Set the switch to ROM and power up, the bootstrap copies itself to RAM, then set the switch to RAM and press reset to sign on. The data bus isolation resistors (R1-R8) are not necessary because the output enable of RAM & ROM are connected to Z80's nRD via the switch.

Bill

File Attachments

- 1) [KIO_testbed.jpg](#), downloaded 466 times
 - 2) [EaZy80_scm.pdf](#), downloaded 463 times
-

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [b1ackmai1er](#) on Thu, 04 Apr 2019 13:29:45 GMT

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Well that's a nice chip. Surprised that it has not shown up in project before.

Regards Phil

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [plasmo](#) on Thu, 04 Apr 2019 14:28:34 GMT

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It is relatively expensive, \$7-\$10 and the address assignments of SIO/CTC/PIO are fixed, so it is probably not compatible with existing Z80 based systems like MSX, ZX80, TR80, etc. It is a cool

chip nevertheless and have a software return-from-interrupt feature that's compatible with Z280. It is rated at 12.5MHz, but I'm curious whether it can run to 22MHz so to be compatible with my 22MHz Z80SBC64.

Bill

Subject: Re: A simple CP/M Z80 SBC without glue logic
Posted by [etchedpixels](#) on Thu, 04 Apr 2019 16:49:09 GMT

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Could the switch be replaced by a simple RC circuit so it powers up in ROM, copies to RAM and spins until the thing flips? Would that still qualify as glueless ?

Subject: Re: A simple CP/M Z80 SBC without glue logic
Posted by [etchedpixels](#) on Thu, 04 Apr 2019 16:56:58 GMT

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plasmo wrote on Thu, 04 April 2019 07:28 It is relatively expensive, \$7-\$10 and the address assignments of SIO/CTC/PIO are fixed, so it is probably not compatible with existing Z80 based systems like MSX, ZX80, TR80, etc. It is a cool chip nevertheless and have a software return-from-interrupt feature that's compatible with Z280. It is rated at 12.5MHz, but I'm curious whether it can run to 22MHz so to be compatible with my 22MHz Z80SBC64.

Bill

I don't think many of the classic mass production systems used such fancy components as the Zilog SIO or PIO. SIO shows up in a few add in cards (Amstrad PCW serial adapter) but the TRS80 has none, the Sinclair systems have none, the Amstrad systems have none except for add in cards. There were cheaper uarts (if even fitted), cheaper ways to do timing, cheaper ways to do PIO (eg the AY-3-8910 gave you PIO as well as sound in one chip)

There was (is ?) a surface mount variant which is a KIO and Z80 on a single chip but afaik that only turned up in embedded gadgetry.

Subject: Re: A simple CP/M Z80 SBC without glue logic
Posted by [plasmo](#) on Thu, 04 Apr 2019 20:58:42 GMT

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So KIO is too late & too expensive as a highly integrated replacement of the earlier Z80 systems. At least it is still available today and a possible candidate for the full-features, fast Z80 new designs. In my short (2 years) exposure to the world of Zx80, I have the feeling that there are greater and greater interests in Zx80 and more people are exploring different ways of using Z80 &

its peripherals. Maybe I'm imaging it, but Retro is now cool?

Bill

PS, Nay! it is the 1/2 bottle of Cabernet Franc talking...

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [wsm](#) on Thu, 04 Apr 2019 21:42:13 GMT

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I agree that some of us are going back to our roots and the Z80 ... it's fun to be able to fully understand all the hardware and software. My "someday" list still includes a small Z84C15 system ... basically the Z80 + KIO at 16MHz. Utsource lists the Z84C1516 (QFP100) for about \$5 but the Z84C13 (basically the same but without PIO) was in PLCC84 form factor. Then again, I already have too many projects on the go!

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [plasmo](#) on Fri, 05 Apr 2019 01:19:13 GMT

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I recalled some discussions on Z84C1516 and had looked into it briefly, but I didn't realize it is available so cheaply from UTSOURCE. This is fortuitous because I recently became interested in the inexpensive acrylic case for Arduino such as this:
<https://www.ebay.com/itm/Acrylic-Case-Shell-Enclosure-Transparent-Protective-Box-For-Arduino-MEGA-2560-R3/122757595> 136

and the 1/2 size even cheaper version like this:

<https://www.ebay.com/itm/Transparent-Acrylic-Case-Shell-Enclosure-Computer-Box-Holder-For-Arduino-UNO-R3/292684035384>

I redesigned the Z80SBC64 for the Arduino Mega case. This is the first prototype.

I need to fix a few mechanical misalignment, but really need to reduce the board size so the CF disk does not stick out so much. I had hoped for a through-hole design, and that may still be plausible with Z80 in PLCC44, but there is another issue: the clear case simply begs for blinking lights. Blinking lights need general purpose I/O, so I either go with CPLD in QFP100 or something else like Z84C1516. In either cases the design will definitely be SMT.

I believe your small Z180 board can easily fit in the Arduino Mega case and possibly the 1/2 size Arduino Uno case.

Bill

File Attachments

1) [Zuno_prototype_top.jpg](#), downloaded 1350 times

2) [Zuno_prototype_side.jpg](#), downloaded 1643 times

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [wsm](#) on Fri, 05 Apr 2019 02:10:54 GMT

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Quote:I believe your small Z180 board can easily fit in the Arduino Mega case and possibly the 1/2 size Arduino Uno case.

I thought about an Arduino case ... briefly. Instead, I've done a new layout to fit into this case - 50mm x 50mm x 19mm or roughly 2" x 2" x 0.6". Same basic specs: 33MHz Z180, 512K flash, 512K or 1MB SRAM, RTC, uSD via SPI @ 25MHz, dual serial and power via USB.

I'm just doing final optimization of the layout. The one issue is with the case's internal mounting pads ... I don't think I can use them as-is.

After this design, I'm thinking it's time to restart my eZ80 project which I started quite a few years ago.

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [etchedpixels](#) on Fri, 05 Apr 2019 10:34:33 GMT

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Would it make sense to use a µSD card and 3.3v convertor instead of CF once you get down to this kind of sizing ? The Raspberry Pi just tucks a µSD on the underside of the PCB.

Pi cases are also another one used for various things and available very cheaply. They are a bit smaller 85x55mm or so but also quite tall (20mm or so above the PCB) because they have to fit in the double USB connectors and RJ45 jack on the end of the Pi.

Subject: Re: A simple CP/M Z80 SBC without glue logic

Posted by [plasmo](#) on Fri, 05 Apr 2019 12:44:19 GMT

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uSD is certainly an option. There are existing adapter with 3.3V regulator and 5V-to-3V buffer for under \$2 like this:

<https://www.ebay.com/itm/Micro-SD-Storage-Board-TF-Card-Memory-Shield-Adapter-Breakout-DIP-Pins-Module/173320605763>

I'm tempted to just have a corresponding female 6-pin socket on board to accept the adapter board so not to fool with the tiny uSD drives.

Bill

File Attachments

1) [uSD_adapter.jpg](#), downloaded 1456 times
