Subject: pdp-10 fpga
Posted by bob98033_yahoo.com on Mon, 15 Oct 2018 16:23:35 GMT
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I did an inquiry with Mr. Conway if he would release the pc artwork and rom file for his PDP-10 fpga running MIT's ITS (Incompatible Timeshare System). Well not only did he send the files he sent me a set of PC blank boards ready to be stuffed! I attached the PC artwork files and ROM binary file. The ROM file is the motorola S3 format as the bin hex format is to large for some rom burner's. Note this FPGA implementation is different from other pdp fpga implementation in that it doesn't use a development board. The reason for that is the 36 bit memory. If access to 36 bit was remapped to fit in 32 bit memory the performance would be terrible. Instead five 512kbyte static rams were used to make 512k X 40 memory (the four most significant bits always low to get 36 bits). There is no Jtag interface. Instead development was done on MAC OSX making a binary image including the code to program the FPGA plus a console program written in PDP-10 assembly. The router files are not in gerber format but in ExpressPCB format. ExpressPCB can convert the file format to gerber format for an additional cost $60 per PCB order. This project uses two PCB so two orders ($120 to convert to gerber format). I have no idea how many people would want a pdp-10 so the conversion to gerber format may not happen.

File Attachments
1) archive.zip, downloaded 432 times
2) archive (1).zip, downloaded 433 times

Subject: Re: pdp-10 fpga
Posted by gkaufman on Mon, 15 Oct 2018 18:07:14 GMT
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I may be able to convert the files at no cost. I'll try tonight.

- Gary

Subject: Re: pdp-10 fpga
Posted by gkaufman on Mon, 15 Oct 2018 18:12:54 GMT
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Try these two...

- Gary

File Attachments
1) syspcb-11.zip, downloaded 398 times
2) x3epcb-03.zip, downloaded 398 times

Subject: Re: pdp-10 fpga
Posted by zamp on Mon, 15 Oct 2018 19:39:20 GMT
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bob98033_yahoo.com wrote on Mon, 15 October 2018 12:23I did an inquiry with Mr. Conway if he would release the pc artwork and rom file for his PDP-10 fpga running MIT's ITS (Incompatible Timeshare System).

Is this David Conroy's FPGA PDP-10? The only real writeup I've seen on it is at http://www.fpgaretrocomputing.org/pdp10x/.

Have you come across any additional information on this FPGA PDP-10? Unless there have been new developments, David was running a version of ITS that he had to modify to use the disk-on-module and serial interfaces that he was using in his PDP-10 clone. Do you know if David has shared his changes to ITS that let it work with his clone?

The idea of building a PDP-10 clone is pretty interesting. If an OS to run on it was available, I'd probably want to build one.

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Mon, 15 Oct 2018 21:54:21 GMT
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I asked David about how to get an image of the OS installed and he sent me on a DVD a copy of the entire pdp-10 development directory from his MAC OSX computer. It includes the source code for the fpga,assembly code for the console,tools to make the ROM image in both motorola S3 and bin hex format, device drivers for aha disk driver,realtime clock,network driver (CHAOS Net the "original arpanet code") and bunch of tools including a special custom emulator that duplicates the functionality of fpga. The last tool he created because there is no FPGA development board and no board debugger. Basically the software development cycle is write source code,compile it,flash result to ROM,plug flash rom into board and turn on the power! His solution is to create an emulator of the FPGA. Right now the tools are written for MAC OSX The DVD does include binary images of flash rom and OS as documented on his site. We can definitely have a PDP-10 running MIT ITS system now... If we wish to modify things then we should update the development environment to run on Linux and windows. Right now I wondering how I should upload the DVD. It is hundreds of megs of source and binary code.

Subject: Re: pdp-10 fpga
Posted by tingo on Tue, 16 Oct 2018 00:33:25 GMT
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Very interesting. Doesn't Xilinx FPGAs have a JTAG interface "built in" to the chip? If so, it wouldn't be hard (well, not too hard) create / wire up a new board and get the bitstream working on that.
Please find a way to put at least source code online (Github / Gitlab repository?, if at all possible.

Subject: Re: pdp-10 fpga
Posted by Andrew B on Tue, 16 Oct 2018 02:56:47 GMT
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Hey all - this sounds like fun, feel free to use the wiki here to collect up information. Let me know if you need help creating a page.

As far as the files, if you want I can create a temporary FTP login for you to upload to and then make the contents available as a folder on the domain here, similar to the legacy wiki archive. We can also do a .zipped version if anyone wants to the grab all of it at once.

Github probably makes a lot of sense for new versions going forward, but best to have a copy stashed here as well.

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Tue, 16 Oct 2018 04:22:20 GMT
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Well right now the three lines for jtag interface are connected to the serial flash rom chip to program the fpga on "reset". The fpga after it is configured then toggles the jtag lines to load the console code from the flash rom to ram (I think high-memory)to start the console/monitor program.

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Tue, 16 Oct 2018 04:44:53 GMT
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I just zipped up the contents of the DVD. The file size is 400 megs since it contains source and binary for everything including a complete ITS file system. I just need a spot to upload it to.

Subject: Re: pdp-10 fpga
Posted by Andrew B on Tue, 16 Oct 2018 05:10:37 GMT
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I PMed some details, go ahead and upload and I'll get it moved to a suitable location & post a link here.

Subject: Re: pdp-10 fpga
Posted by will on Tue, 16 Oct 2018 20:25:09 GMT
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"I have no idea how many people would want a pdp-10"

Well I would!!

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Tue, 16 Oct 2018 23:29:19 GMT
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here is the pictures of the two blank PC boards provided by Gary Conway. Someone please compare to gerber files generated by Gary to verify if correct.

File Attachments
1) DSCN0361.JPG, downloaded 607 times
2) DSCN0362.JPG, downloaded 550 times

Subject: Re: pdp-10 fpga
Posted by pbirkel on Wed, 17 Oct 2018 09:51:15 GMT
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"I have no idea how many people would want a pdp-10"

I would as well!!

Subject: Re: pdp-10 fpga
Posted by gkaufman on Wed, 17 Oct 2018 17:33:25 GMT
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bob98033_yahoo.com wrote on Tue, 16 October 2018 16:29here is the pictures of the two blank PC boards provided by Gary Conway. Someone please compare to gerber files generated by Gary to verify if correct.

As long as the original express pcb files are accurate, the converted files should be identical.

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Wed, 17 Oct 2018 20:38:45 GMT
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I was comparing the express pcb file conversion to sbc6120 kicad/gerber file and I don't see a Excellon drill file ... *drl. I don't know too much about gerber files is a drill file necessary?

Subject: Re: pdp-10 fpga

Posted by gkaufman on Wed, 17 Oct 2018 22:30:53 GMT
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I'm no expert on Gerber files (by a long shot), but there appears to be a drill file (.xln).
The files appear to load nicely using Gerbv.

I exported the gerbers as configured for OSH Park, but most other vendors should be fine with these files.

- Gary

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Fri, 19 Oct 2018 12:28:51 GMT
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gkaufman:
The syspc-11.xln and x3epcb-03.xln report errors when I try to open the files under Gerbv.
"Unexpected symbol" is displayed in a dialog box and no layer is drawn...Please check.

Subject: Re: pdp-10 fpga
Posted by gkaufman on Fri, 19 Oct 2018 13:19:43 GMT
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Both open and display fine for me using Version 2.6A of Gerbv.

Extract the .zip into a directory
F)ile, O)pen Layers
  browse to the files...
  ^A to select all
O)pen
  you can then uncheck or check each layer to view.

I'll upload to OSHPark in a few minutes and post a link.

- Gary

bob98033_yahoo.com wrote on Fri, 19 October 2018 05:28gkaufman:
The syspc-11.xln and x3epcb-03.xln report errors when I try to open the files under Gerbv.
"Unexpected symbol" is displayed in a dialog box and no layer is drawn...Please check.

Subject: Re: pdp-10 fpga
Posted by gkaufman on Fri, 19 Oct 2018 13:29:09 GMT

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OSHPark links for ordering (fairly costly):

SYSPC-11: https://oshpark.com/shared_projects/CpW7PMc1

X3EPCB-11: https://oshpark.com/shared_projects/X3VYEDr2

- Gary

Subject: Re: pdp-10 fpga
Posted by Andrew B on Fri, 19 Oct 2018 14:21:43 GMT
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The archive file from bob is now available at:
http://www.retrobrewcomputers.org/fpga-pdp10-archive/v3arch.zip

Subject: Re: pdp-10 fpga
Posted by pbirkel on Fri, 19 Oct 2018 17:48:40 GMT
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Said Gary: "OSHPark links for ordering (fairly costly)"

Rahtah! I'd support a group-buy from a (much) more cost-effective supplier. Anyone else here so inclined?

Subject: Re: pdp-10 fpga
Posted by ale500 on Sat, 20 Oct 2018 06:11:36 GMT
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The FPGA alone is 36 a pop . There are nice Spartan 6 modules (from aliexpress) with a 16 k LE fpga and enough pins for the RAM and IDE, I think. One could use that, the baords are like 17 € or so.

https://de.aliexpress.com/item/Spartan6-entwicklungsboard-XI
LINX-FPGA-SDRAM-Spartan-6-tr-gerplatte-XC6SLX16/32851234772.
html?spm=a2g0x.search0104.3.9.7c374763DUa5YJ&transAbTest
=ae803_4&ws_ab_test=searchweb0_0%2Csearchweb201602_1_103
20_10065_10068_318_10547_319_10548_317_10696_450_10084_10083
_10618_452_535_534_10304_10307_533_10820_532_10821_10302_204
_10843_10059_10884_323_10887_5023911_100031_10319_320_572761
1_321_322_10103_448_449%2Csearchweb201603_45%2CppcSwitch_0&a mp;a
mp;algo_pvid=6f30735e-8d64-4bcc-bb1b-1f5bc6bc2632&algo_e

xpid=6f30735e-8d64-4bcc-bb1b-1f5bc6bc2632-1

There are two variants one with SDRAM and one with DDR3 DRAM. SDRAM is easier to get to work than DDR3. The only drawback is that the programming is not a standard connector (not a 2x7 2.0 mm header), but a single row od 2.54 mm spaced pins, it works anyways but not all programmers have the flying wires. It could be a possibility.

File Attachments

1) XC6SLX16__Schematic.pdf, downloaded 330 times

Subject: Re: pdp-10 fpga
Posted by ale500 on Sat, 20 Oct 2018 06:35:01 GMT
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I did a quick test synthetizing it for a nother FPGA to size the amount of logic needed (Target MachXO2-7000), it needs 108 pins plus one for a LED, the Spartan6 board has 108 free pins plus some leds and pushbuttons.

Design Summary
  Number of registers: 1115 out of 7209 (15%)
    PFU registers: 1022 out of 6864 (15%)
    PIO registers: 93 out of   345 (27%)
  Number of SLICEs: 2721 out of 3432 (79%)
    SLICEs as Logic/ROM: 2310 out of 3432 (67%)
    SLICEs as RAM: 411 out of 2574 (16%)
    SLICEs as Carry: 109 out of 3432 (3%)
  Number of LUT4s: 5173 out of 6864 (75%)
    Number used as logic LUTs: 4133
    Number used as distributed RAM: 822
    Number used as ripple logic: 218
    Number used as shift registers: 0
  Number of PIO sites used: 109 + 4(JTAG) out of 115 (98%)
  Number of block RAMs: 0 out of 26 (0%)
  Number of GSRs: 1 out of 1 (100%)

Looks promising !!!

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Mon, 22 Oct 2018 18:26:01 GMT
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Well my first attempt at soldering the 208 pin fpga ended in failure. I had to use "chip quik" to remove the IC. Now of course several of the pins are damaged so I need a new replacement. At $36 a pop I it maybe time to shelf the PDP-10x the project unless you know someone in this forum who has experience soldering SMD of this many pins... 52 pins per side
of one inch length. Notice before I started I got one of the smd "trainer" soldering kit but the IC is only 44 pin flat pack. The pin density of this fpga is much higher than a qfp44 package that comes in the trainer. I have seen "you tube videos" of using a heat gun to solder in a smd chip so maybe that is how you do it. Any suggestions out there ?

Subject: Re: pdp-10 fpga
Posted by will on Mon, 22 Oct 2018 19:03:54 GMT
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My recommendation for SMD soldering is always: Use a LOT of liquid flux. Flux and a good soldermask work together and the surface tension of the molten solder allows it to end up where you need it to be. If you have too much solder use solder braid (again with a lot of liquid flux) to remove the excess.

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Mon, 22 Oct 2018 20:14:19 GMT
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I forget one detail ... The board I am using from Conway has NO SOLDER MASK. Another item is pad on the board is very short basically the length of the pad on the end IC. What is your suggestion now?

Subject: Re: pdp-10 fpga
Posted by will on Mon, 22 Oct 2018 21:01:23 GMT
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Ah maybe the PCB was designed for reflow soldering (you're approaching the limits of my SMD knowledge!). I'm guessing the idea was to put solder paste on the board with a mask or with a syringe, then pop the chip on top, then heat up the whole ensemble.

The PCB doesn't look too horrendously complicated -- maybe you could just make a new version in KiCAD with pads suitable for hand soldering and send it off to a prototyping service which would make boards with a soldermask for you?

Subject: Re: pdp-10 fpga
Posted by jcoffman on Mon, 22 Oct 2018 22:38:37 GMT
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My technique for soldering the PQFP-132 386EX went as follows:

A. Coat the PQFP board pads with liquid flux. IMPORTANT.
B. (optional) Tin the board with a flat tip iron with MINIMUM solder. This is not necessary if the HASL layer has enough solder to attach the chip pins.
C. Coat the bottoms of the PQFP pins with liquid flux.
D. Position the PQFP; tack down corners with a DRY (solder-free) flat or wedge tip iron. Re-check positioning constantly.
E. Finish heating all of the pins with the DRY flat or wedge tip iron until all pins pass visual inspection under a jewelers loupe (8X) magnifier.
F. (optional) If you have a low voltage (<3v) tester, buzz out the connections with straight pins used as probes. This is tedious.

--John

Subject: Re: pdp-10 fpga
Posted by ale500 on Tue, 23 Oct 2018 17:37:19 GMT
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I did solder a QFP208 once, a Spartan2. It was kind of difficult. I did also go for lots of flux, flat tip iron, an solder the corners first. I still have a second Spartan2 that got unused...
I ordered another Spartan6 board, I think it is a better option, the FPGA is already soldered and has 0.1" headers.

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Wed, 07 Nov 2018 16:52:24 GMT
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I just ordered a set of ten cpu/system boards from "dirtypcs" for $133. This is much cheaper than OSHPark price of $300 for one set. I chose them because of message of the builders having good luck with "dirtypcs". The vendor is in Hong Kong so I will know in the month if I made a good purchase or not.

Subject: Re: pdp-10 fpga
Posted by ale500 on Tue, 20 Nov 2018 19:03:32 GMT
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I got today a SDRAM controller in verilog working, at least in the simulator. The pdp10x simulates without problems too. My target will be the Spartan6 on the board I posted about earlier. As soon as something works I'll poste it in the wiki page, maybe we can build something around a cheaper setup. The boards you got (or are going to get are sitting in the states aren't they ?, postage and tax would probably cost as much as ordering new sets from some smart prototypes or similar... I think.

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Tue, 04 Dec 2018 06:29:57 GMT
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Today I received from Hong Kong a set of ten cpu/main boards. I also bought six fpga's and six flash spi's. One of the flash IC's is SMD the other five are DIP.

File Attachments
1) DSCN0404.JPG, downloaded 2291 times
2) DSCN0405.JPG, downloaded 2327 times
3) DSCN0406.JPG, downloaded 2273 times

Subject: Re: pdp-10 fpga
Posted by bob98033_yahoo.com on Wed, 05 Dec 2018 14:30:42 GMT
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PDP-10x board inventory:
SYSPC-11 and X3EPCB-11 $20 for the set. SYSPC-11,X3EPCB-11,fpga and flash SPI $40

Subject: Re: pdp-10 fpga
Posted by pbirkel on Wed, 05 Dec 2018 14:57:57 GMT
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bob98033_yahoo.com wrote on Wed, 05 December 2018 06:30PDP-10x board inventory:
SYSPC-11 and X3EPCB-11 $20 for the set. SYSPC-11,X3EPCB-11,fpga and flash SPI $40

I'm (still) interested in your mini-kit. I'm located in Maryland.

Not looking forwards to soldering the ICs; still a thru-hole guy. Gotta learn sometime I guess ...

THX!

Subject: Re: pdp-10 fpga
Posted by djmartins on Sat, 09 Feb 2019 16:53:30 GMT
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I have a MiSTer board and this would make a great core for it!
It already has the MultiComp and a PDP-1 on it and a lot of other cores.
The dev would need to release the FPGA source code though, or write a core for MiSTer.

Subject: Re: pdp-10 fpga
Posted by gerryk on Wed, 07 Aug 2019 12:00:47 GMT
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I am looking at how feasible this might be. One thing that will definitely need some thought is how to handle the RAM.
RAM on the MISTer is a single SDRAM module... probably 32bit. The RAM for the PDP10/x is 5x512k SRAM modules, set up so that the 40 data bits are provided by the 5 modules directly map to the 36 bits required by the PDP10/x, with the high 4 bits pulled low. This approach would not be possible in the SDRAM module, since there are only 32 data bits, so some code or other translation would be needed to handle the 1 PDP word -> 2 SDRAM word alignment.
Alternatively, a similar SRAM module could be made up to provide the necessary RAM in the same way that Dave Conway has implemented it.

Ok, just saw this:

I got today a SDRAM controller in verilog working, at least in the simulator. The pdp10x simulates without problems too. My target will be the Spartan6 on the board I posted about earlier. As soon as something works I'll poste it in the wiki page, maybe we can build something around a cheaper setup. The boards you got (or are going to get are sitting in the states aren't they ?, postage and tax would probably cost as much as ordering new sets from some smart prototypes or similar... I think.

// Gerry

Subject: Re: pdp-10 fpga
Posted by gerryk on Wed, 07 Aug 2019 12:13:08 GMT
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ale500 wrote on Tue, 20 November 2018 11:03I got today a SDRAM controller in verilog working, at least in the simulator. The pdp10x simulates without problems too. My target will be the Spartan6 on the board I posted about earlier. As soon as something works I'll poste it in the wiki page, maybe we can build something around a cheaper setup.
Do you have anything further on this?

Subject: Re: pdp-10 fpga
Posted by robg on Wed, 21 Aug 2019 14:41:52 GMT
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Hello PDP10 Fans,

I've gone down the path of reimplementing Conroy's PDP10/X System Board in Kicad 5. For the FPGA, I'm using a board from Waveshare [1] which uses the same Xilinx Spartan 3E FPGA as Conroy's design. This board uses 2mm pin spacing instead of the usual 2.54mm, but hopefully will be easier to solder than a 0.5mm pitch PQFP. :)

I've made a few changes as compared to Conroy's original system board:

5V Power via a barrel jack instead of a Molex connector
Clocks are derived from the 50 MHz oscillator on the FPGA board instead of using discrete oscillators.
TTL (3.3V) serial, removing the MAX232 chips
Conroy uses one SPI Serial ROM for both FPGA configuration and the PDP10 ROM. I'm using the ROM on the FPGA board for config only, with a separate SPI ROM on the system board for the PDP10 ROM. This minimizes Verilog changes.

Boards should be arriving in the next couple of days. I'll probably load up a Multicomp system to do basic hardware checkout before tackling Conroy's ITS.

[1] https://www.waveshare.com/product/fpga-tools/xilinx/core/cor e3s500e.htm

-- Rob

File Attachments

1) PDP10X.png, downloaded 1833 times

Subject: Re: pdp-10 fpga
Posted by gerryk on Thu, 22 Aug 2019 14:39:19 GMT
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Very interested to see how this works out Rob.

Subject: Re: pdp-10 fpga
Posted by robg on Sat, 24 Aug 2019 00:55:24 GMT
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Thanks Gerry.

Well, the boards have arrived, without silkscreen :cry:. Guess JLCPCB decided I needed a little bit more challenge when assembling the board. The silkscreen is clearly there on the Gerber viewer on their website, so I guess this is some sort of production mistake.

I've assembled the power circuit (barrel jack, 3.3V regulator, some caps) and added the pin sockets for the FPGA board. Here you can see the FPGA running the little LED demo program that it ships with, so at least it is getting power.

The system board has a couple of LEDs on it, so I will download some Verilog to blink those next.

-- Rob

File Attachments
1) FPGA_LEDS.GIF, downloaded 1620 times

Subject: Re: pdp-10 fpga
Posted by ale500 on Sun, 25 Aug 2019 06:29:15 GMT
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I haven't made much more progress yet since a friend of mine borrowed the board I bought for this project :(. I have some other possible targets, like a DE0-Nano and a DE10-Lite, but they are Altera-based boards.
Anyways I am really liking Rob's approach of using a Spartan3E module (you can get off aliexpress :))
@Rob: would you post your Kicad or gerber files so we could also order some boards ?

Subject: Re: pdp-10 fpga
Posted by robg on Tue, 08 Oct 2019 01:48:36 GMT
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Well, it time for an update on this. I've got all of the hardware basically working. I can successfully telnet into the board via its network interface (see last screenshot), and the serial console works fine. So the FPGA clocking, RAM, Serial ROM and IDE/CF interface all checkout. The only Verilog I've changed is around generating the clocks from the 50 MHz oscillator on the FPGA board.

The DS1337 RTC chip seems to work from a hardware perspective in that I can write to it, read those values from it, and see that the values stored are retained across a power-cycle via battery. But I don't understand the values that ITS is writing to it, and ITS does not seem to read from it at boot time, so I have to manually set the time on a reboot.

On the network side, I can't telnet out (at least) because the TELNET binary is missing on the disk image I have, and some of the CHAOSNET stuff that Conroy shows on his screenshots on his writeup does not work for me. But I don't think these are hardware problems, but rather software ones and/or my lackof understanding how to get them to work.

Also for reasons as yet unknown the usual ITS shutdown sequence does not work.

I made a few hardware blunders on this prototype, so I'm doing another spin of the board, while making some changes to make it usable as a Multicomp system also (adding an SD card interface for sure, maybe VGA and PS/2 by reusing the pins of Ethernet interface that aren't usable in a Multicomp system).

Once I get this next iteration of the board debugged, I'll post the schematics, KiCad files, etc. on a builderpage.

Conroy has a few screenshots on his writeup as he debugged his original board. Here are some of the equivalent screenshots for my version of the board.

Initial boot, zeroing out and displaying some memory. This shows basic PDP10 instructions running to get to this point.

Depositing some code via the ROM monitor, then running it.

Booting Conroy's customized version of the Incompatiable Timesharing System (ITS).

A directory listing.

Telneting in the board, logging in, checking the time, listing some files, and running ":peek", which is like Unix's top or ps. It shows me logged in as "ROBG" on the console, and "ROBG2" via the network.

Rob

File Attachments

1) PDP10X_01.png, downloaded 1395 times
2) PDP10X_02.png, downloaded 1319 times
3) PDP10X_03.png, downloaded 1417 times
4) PDP10X_04.png, downloaded 1412 times
5) PDP10X_05.png, downloaded 1414 times

Subject: Re: pdp-10 fpga
Posted by robg on Tue, 08 Oct 2019 01:53:54 GMT
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And here's a picture of the assembled board:

As a computer history enthusiast, it's been great to have an excuse to dive into the worlds of PDP-10 and the ITS operating system, which I probably would have never done otherwise.

Rob

File Attachments

1) PDP10X_06.jpg, downloaded 1429 times

Subject: Re: pdp-10 fpga
Posted by gerryk on Tue, 08 Oct 2019 17:20:22 GMT
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Great work Rob!

Subject: Re: pdp-10 fpga
Posted by hsnewman on Wed, 16 Oct 2019 17:38:08 GMT
View Forum Message <> Reply to Message

Rob, will these boards run Tops-10 or 20?

Subject: Re: pdp-10 fpga
Posted by robg on Wed, 16 Oct 2019 18:42:33 GMT
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Hi,

These operating systems would have to be ported to the board, as Conroy did for ITS. I don't know how much work that would be. Conroy wrote ITS drivers for his custom MMU, the IDE interface, Ethernet interface, and the RTC chip. You might followup in this thread on alt.sys.pdp10 where PDP10 experts could chime in on how much work would be involved if you're interested: https://groups.google.com/forum/#!topic/alt.sys.pdp10/wgEN2t DTmKg

Rob

Subject: Re: pdp-10 fpga
Posted by hsnewman on Thu, 17 Oct 2019 14:00:12 GMT
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Do you still have any boards for sale?

Subject: Re: pdp-10 fpga
Posted by robg on Thu, 17 Oct 2019 22:49:08 GMT
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I haven't made any boards available. This first set of boards has several errors (missing pull up resistors, power distribution errors, missing silkscreen). I'm working on another spin of the board to fix these issues and to make the board more Multicomp compatible. When I've got that done, I will make the schematics and Gerbers available and will probably have a handful of boards available.

Rob

Subject: Re: pdp-10 fpga
Posted by hsnewman on Thu, 17 Oct 2019 23:05:16 GMT
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Can you put me on the list when you complete the new version?
Thanks,
Harris

Subject: Re: pdp-10 fpga
Posted by robg on Fri, 18 Oct 2019 21:41:09 GMT
View Forum Message <> Reply to Message

Sure thing.

Rob

Subject: Re: pdp-10 fpga
Posted by gerryk on Mon, 13 Jan 2020 10:57:50 GMT
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Hi Rob...
I'm wondering if you have made any progress with this?
No pressure, btw.
/ Gerry

Subject: Re: pdp-10 fpga
Posted by robg on Wed, 15 Jan 2020 04:49:18 GMT
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Hi Gerry,

Thanks for asking. I'm waiting for what I hope to be the final version of the board to arrive tomorrow. I'm expecting to get this new board assembled this weekend and have a more complete update sometime next week. Getting close.

Rob

Subject: Re: pdp-10 fpga

Posted by gerryk on Wed, 11 Nov 2020 17:14:33 GMT
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I git a board for this project from Rob back in February, and between COVID related delays and various other impediments, it has taken me until now to get it done. I have 99% of the board done, with only the crystal for the RTC and the ethernet adapter remaining to fit, and they are in the mail, so I'm rapidly approaching the point of initial power-up.

Has anyone else tried this project, whether on Rob's board or their own?

I do have a couple of questions...,

1. Is there a bitstream that I can just blast onto the FPGA, or do I need to download Quartus or something to synth it from the VHDL?
2. Is there an image with Conroy's ITS I can just image to the CF card? I can see what looks like the files for ITS, but I doubt the PDP10 can understand FAT32, so I guess I need an image of a PDP10 disk, right?

Any help gratefully received.

This is the board, BTW...

Subject: Re: pdp-10 fpga
Posted by robg on Thu, 12 Nov 2020 03:49:48 GMT
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gerryk wrote on Wed, 11 November 2020 09:14I git a board for this project from Rob back in February, and between COVID related delays and various other impediments, it has taken me until now to get it done. I have 99% of the board done, with only the crystal for the RTC and the ethernet adapter remaining to fit, and they are in the mail, so I'm rapidly approaching the point of initial power-up.

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Any help gratefully received.

This is the board, BTW...

Hi Gerry,

You're the only person I sent a board to. I've since reworked to the board to use a Spartan-6 FPGA board. The Spartan-6 is not only larger, allowing for more system possibilities, it is cheaper too. I've almost got the revised board ready for anyone who might be interested.

Anyway, I'll continue to support your use of the Spartan-3E version. Answers to your questions:

1. I've attached a dump of the serial ROM used with the board. This binary file contains the FPGA bitstream and the 1K-word PDP10/X ROM image. Just burn this to the W25Q32JV and you should boot into the ROM monitor immediately on power-up.

2. The archive hosted by this site at http://www.retrobrewcomputers.org/fpga-pdp10-archive/v3arch. zip contains the necessary disk image at v3arch/disk/sim10x.disk. Write that to your Compact Flash card.

Let me know if you have more questions...

Rob

File Attachments

1) pdp10x_spartan3_spi_rom.bin, downloaded 142 times

Subject: Re: pdp-10 fpga
Posted by gerryk on Thu, 12 Nov 2020 19:20:00 GMT
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Awesome! Many thanks. Will give it a try over the next day or two.

Subject: Re: pdp-10 fpga
Posted by hsnewman on Mon, 16 Nov 2020 21:40:40 GMT
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Rob,
When will you update the files to be for the Sparten 6? Also, does the pdp10x have the ability to multiboot under multicomp? Finally, are you in Austin, I'm in Cedar Park...

Subject: Re: pdp-10 fpga
Posted by robg on Tue, 17 Nov 2020 05:37:29 GMT
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Hi Harris,

I hope to update the files for the Spartan-6 version in the next couple of weeks. It won't be on the Wiki, probably GitHub instead, as I can't reset my wiki password with the forum email not working. The stuff I have on my builderpage is for the Spartan-3 version, frozen in time.

I'm not sure exactly what you mean by "ability to multiboot," but the board can run both Multicomp and PDP10/X, though switching between them is a manual process of using the Xilinx ISE/iMpact tool to program the FPGA or serial ROM each time you want to switch. And as a bonus :) because the QMTECH FPGA board I'm using has SDRAM, the system will run Will Sowerbutt's socZ80, which Alan Cox once referred to as one of the fastest non-software-emulated Z80 system he's used.

And yep, I'm in Austin, on the southwest side. Howdy neighbor.

-- Rob

File Attachments

1) IMG_1104.jpg, downloaded 821 times

Subject: Re: pdp-10 fpga
Posted by djmartins on Sun, 22 Nov 2020 06:10:37 GMT
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How about porting it to the MiSTer FPGA system?
Already a few retro machines on MiSTer including a PDP-1 and
would love to see more DEC machines on it.

Subject: Re: pdp-10 fpga
Posted by gerryk on Fri, 26 Mar 2021 10:09:28 GMT
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robg wrote on Wed, 11 November 2020 19:49
1. I've attached a dump of the serial ROM used with the board. This binary file contains the FPGA bitstream and the 1K-word PDP10/X ROM image. Just burn this to the W25Q32JV and you should boot into the ROM monitor immediately on power-up.
Hi Rob

Got a little sidetracked over the last few months, but finally got round to trying this. I hvae an SPI EPROM flashed with the attached image (and verified by reading off and diffing against the original binary). The FPGA starts up with the default LED flashing image, but that's as far as it goes.
If I connect a serial terminal to the TTY, I just get a series of NULLs.

I have traced the SPI lines from the EPROM to the FPGA headers, and all seems fine.

I guess I am missing something obvious but can't think what it might be.

Subject: Re: pdp-10 fpga
Posted by robg on Sat, 27 Mar 2021 04:27:43 GMT
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gerryk wrote on Fri, 26 March 2021 03:09robg wrote on Wed, 11 November 2020 19:49
1. I've attached a dump of the serial ROM used with the board. This binary file contains the FPGA bitstream and the 1K-word PDP10/X ROM image. Just burn this to the W25Q32JV and you should boot into the ROM monitor immediately on power-up.
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Got a little sidetracked over the last few months, but finally got round to trying this. I hvae an SPI EPROM flashed with the attached image (and verified by reading off and diffing against the original binary). The FPGA starts up with the default LED flashing image, but that's as far as it goes.
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I have traced the SPI lines from the EPROM to the FPGA headers, and all seems fine.

I guess I am missing something obvious but can't think what it might be.
Hi Gerry,

In that November message, I incorrectly suggested that the Spartan-3 FPGA configuration is loaded from the SPI ROM on the system board, but that's not right. On the Spartan-3 version you have, the SPI ROM on the system board provides the PDP10/X boot code, while there's a separate ROM on the FPGA daughterboard that provides the FPGA bitstream. So you''ll need to use the Xilinx ISE tools to program the FPGA. I'll need to send you a bitstream. (On the Spartan-6 version, it is the case that there's one ROM that stores the FPGA config and the PDP10/X boot code.)

-- Rob

Subject: Re: pdp-10 fpga
Posted by gerryk on Sat, 27 Mar 2021 10:59:41 GMT
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Ah right... that makes sense.
I do have an Xilinx JTAG to flash the ROM in the FPGA, so no problems there.
Thanks
Gerry

Subject: Re: pdp-10 fpga
Posted by robg on Sat, 27 Mar 2021 16:36:36 GMT
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Hi Gerry,

Here's the bitstream file you need to load into the FPGA's config ROM (xcf04s) via Xilinx's iMPACT tool.

-- Rob

File Attachments
1) kx.mcs, downloaded 123 times

Subject: Re: pdp-10 fpga
Posted by gerryk on Mon, 29 Mar 2021 13:29:42 GMT
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Thanks Rob...
That worked... up to a point. I have an image on the FPGA EPROM that boots to a different LED pattern L1, L2 light up along with Power and Flag. But that's as far is it goes.
Would you have any suggestions?
/ Gerry

File Attachments
1) 20210329_103717.jpg, downloaded 661 times

Subject: Re: pdp-10 fpga
Posted by gerryk on Mon, 29 Mar 2021 16:51:09 GMT
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Incidentally... just came across this: https://github.com/aap/fpdpga
Both PDP6 and PDP10 implementations. Not quite as advanced as your/Conroy's implementation in that no mass storage yet, but still interesting.

Subject: Re: pdp-10 fpga
Posted by robg on Mon, 29 Mar 2021 18:02:10 GMT
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I haven't looked at that PDP10 FPGA. There are several floating around on the internet.

BTW, I sent you a couple of private messages. I suggest we move the debug of your board to

email for convenience.

-- Rob

Subject: Re: pdp-10 fpga
Posted by robg on Tue, 30 Mar 2021 05:03:49 GMT
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Ok, let's simplify things a bit. I've attached 'kx_bram.bit' which is the PDP-10/X bitstream that doesn't use the config ROM nor the SPI ROM. The Xilinx tool will write this via JTAG to the FPGA's SRAM. Note, in this mode, the FPGA will forget the bitstream when the power is off.

After you program this into the FPGA, you should see something on the serial port (set to 9600 baud 8N1). Hopefully you'll see

ROM10X.85
?RTC ERR
.

Before doing this, you might find it helpful to reprogram the FPGA config ROM with the default LED demo bitsteam, which I've also attached. I find this useful to easily tell the difference between a default bitstream and a programmed bitstream.

If load 'kx_bram.bit' works, then you can load 'kx_bram.mcs' also attached, into the FPGA config ROM. Program the ROM, turn off the board, then turn it back on. You should see the same serial port output. If that works, that will be the permanent bitstream for the board. The SPI ROM will no longer be used at all.

Let me know how it goes...

-- Rob

File Attachments
1) kx_bram.mcs, downloaded 117 times
2) LED4.mcs, downloaded 117 times
3) kx_bram.bit, downloaded 112 times

Subject: Re: pdp-10 fpga
Posted by djmartins on Sat, 10 Apr 2021 22:03:30 GMT

https://github.com/MiSTer-devel/Main_MiSTer/wiki

Check this system out, it is ripe for more DEC retro cores.