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Subject: Re: Gryphon 68030

Posted by [yoda](#) on Mon, 13 Jun 2016 01:06:26 GMT

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lynchaj wrote on Sun, 12 June 2016 19:16Hi

Today has been a good day. Got outside, did stuff with the family, and got a chance to work on the Gryphon schematic and PCB.

Here is an updated KiCAD EDA file set to include an updated schematic and initial PCB layout. Doing the PCB layout was highly educational and I discovered numerous errors in the part footprints and in my schematic as well.

Regarding the CPLDs; since we are going down the programmable logic path anyway I have a suggestion. Rather than consolidate the 7 PALs into one CPLD how about focus on eliminating the 13 74LSxxx glue logic chips instead? If you look at the board, there are a whole bunch of miscellaneous logic chips in the center left of the board which are going to be a pain for trace routing. If you want to save PCB space take a look at them first. Maybe two CPLDs to consolidate the PALs and the 7LSxxx glue logic.

Thanks

Andrew Lynch

I would not propose to consolidate them all. I would leave the DRAM glue one alone as we barely got that one to work (the original equations were for a dialect of equations that were not well documented). I would move the chip decodes into the CPLD for sure as well as some of the remap of ROM after the Reset Trampoline. I would also bring the 4 address lines that you discovered that are not used into the CPLD to fully qualify the Chips selects as the original design ignored them so all chip selects mapped into multiple addresses because of this which is not very nice in the end. I would probably include the DSACKs here as well - so we would consolidate 4 GALS into one CPLD. Looks like Coprocessor decode would also go into as well as it mostly address lines that go into it which are already going into the Chip decodes so 5 into 1 and there would be 2 left plus the Interrupt one you don't have - I will have to look at the equations to see if that would be standalone or consolidated.

Dave

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