Subject: Re: Gryphon 68030
Posted by yoda on Sun, 12 Jun 2016 15:07:36 GMT
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lynchaj wrote on Sun, 12 June 2016 09:13Hi Dave
OK looks good to go with the CPLD. I like the idea of some spare logic capacity since the 512K SRAM would require a bit of decoding and swap logic to get it to replace the Flash on command. My concern is to keep the project focused and not introduce too many changes at once or it will blow up into massive complexity. Lets get what we have working first and then modify something we know works. The bus, more advanced CPUs, DMA, etc. can wait for now.

The SRAM does not replace the Flash. Flash is mapped at the top of memory then the SRAM is mapped directly below it. DRAM is mapped from 0. The SRAM can be used for stack, variable scratch space and buffers.

Quote:
While others are working on reviewing the schematics, making the CPLD changes, etc. I will start on replicating the Gryphon 1.0 PCB layout so we can verify part footprints. There will have to be some differences because the Gryphon specified parts like the stacked 9 pin dual male DB connectors which are unobtainium in KiCAD. Those will have to be replaced with single male DB9s.

Thanks

Andrew Lynch

PS, BTW do we really need 512KB Flash and 1024KB SRAM just to boot this thing? How about a 32KB EEPROM and a pair of 32KB skinny SRAMs instead? Pull the rest of the initialization data from external stores. It is something to consider and may simplify this design a bit -- possibly a 32KB EEPROM for boot only to bring in the DRAM and swap out the EEPROM for an all DRAM system.

Yes keep the size. Paul and I did a very nice curses monitor that uses more than 32k and is/was growing.