Hi Will

Paul and I had talked about the ROM at 0 in the Gryphon and that was a planned change in next version - it is pretty simple to do. The problem with 68040 and 060 is there is no dynamic bus sizing support so things now all devices have to be 32 bit wide (Rom, ram, I/O). There are ways around it like the 68360 and 68150. Andrew and I played with the 68360 a while ago and might be time to resurrect it. It is definitely not for the faint of heart to program (there are so many registers and modes for the device). It does provide some useful I/O and a dynamic memory controller. Knowing what I know now from the Gryphon bring up and other things I think it might be a useful device to bring back (I guess I will have to dust off my proto board and remember where I left off). Andrew's and my intentions were to eventually marry this to a 68040 - that might be the next direction after getting a core Gryphon running smoothly.

I have also thought about FPGA's in the design but the drawback is that you have to "download the design" into the FPGA before you can use, so if you don't have some way of boot code sequence, you have a hard time using them for glue logic.   I got a bunch of Altera Max 7128slC84's which are relatively cheap from UtSource and they are 5 volt tolerant versions and the JTAG pod for Altera is reasonably cheap as well - can be had on eBay for less than 20 dollars normally. The software is free and runs on Windows and Linux so that is nice as well. I must admit I have not tried them out yet but I think it is pretty straight forward to use them.

The high resolution display is a real issue because getting beyond 800x600 is non trivial. An FPGA might be the route to use for that. I plan on on experimenting with a DE0 nano to do something like that. So many projects in the queue.

I am somewhat excited as this project can expand in many different directions going forward

Dave