Subject: Re: A simple CP/M Z80 SBC without glue logic
Posted by wsm on Fri, 15 Mar 2019 17:15:02 GMT
View Forum Message <> Reply to Message

Quote:Looking up the datasheet of AS6C1008, I see the OE is "don't care" when WE is asserted for write operation, so I don't need to negate OE for write. Whew!
I learn (or remember) something new every day. Although I've looked at various memory chip's decoders, I wasn't paying attention to the output tri-state disable when WE* is active.

I still think you'll have some data bus contention with the RAM unless OE* is connected to RD*. The Z80 WR* signal goes active roughly 1T after MREQ* goes active (#8 to #30) and thus the RAM will first be in read mode if OE* is tied low. However, the Z80 Dout goes active a minimum of 20ns before WR* (#29). The AS6C1008 will be WE# controlled and it's Dout will still be driven for tWHZ (max 20ns) after WE#. Looks to me like the overlap is a minimum of about 32ns for a 12.5MHz Z80 and possibly a lot longer.