Subject: Re: A simple CP/M Z80 SBC without glue logic
Posted by plasmo on Fri, 15 Mar 2019 16:11:09 GMT
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wsm wrote on Fri, 15 March 2019 09:47Plasmo: Tying MREQ* to CS* of the RAM and ROM would work but the switching of OE* might require some glue. At power-on the ROM's OE* needs to be low and the RAM's high which can be done via pull-down / pull-up. After the copy, the ROM's OE* can go high from a KIO port. HOWEVER, the RAM's OE* needs to be tied to RD* or possibly NOT WR* after the switch to avoid bus contention during RAM writes i.e. simultaneous RD* and WR* from/to RAM.

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Looking up the datasheet of AS6C1008, I see the OE is "don't care" when WE is asserted for write operation, so I don't need to negate OE for write. Whew!

Bill