Subject: Re: A simple CP/M Z80 SBC without glue logic
Posted by wsm on Fri, 15 Mar 2019 15:47:18 GMT
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Plasmo: Tying MREQ* to CS* of the RAM and ROM would work but the switching of OE* might require some glue. At power-on the ROM's OE* needs to be low and the RAM's high which can be done via pull-down / pull-up. After the copy, the ROM's OE* can go high from a KIO port. HOWEVER, the RAM's OE* needs to be tied to RD* or possibly NOT WR* after the switch to avoid bus contention during RAM writes i.e. simultaneous RD* and WR* from/to RAM.

etchedpixels: The KIO's CS* could be tied to a high address bit and that should work including if interrupts are enabled i.e. IORQ* active but RD* and WR* inactive. If the KIO is the only I/O device then it might be simpler to just tie CS* low and let the KIO decode IORQ*, M1*, RD* and WR*.