Subject: Re: Gryphon 68030
Posted by norwestrzh on Tue, 21 Mar 2017 17:22:20 GMT
View Forum Message <> Reply to Message

1) I've read that the 68K takes minimum of 4 clock cycles for memory access. If the ROM/SRAM on the board has an access time roughly equal to the clock period, is there ever any reason to delay DTACK? Slow I/O devices may need some delays but fast ROM/SRAM should be ready long before the 68K is. Am I missing something?

If you can find a copy of the Wilcox 68000 book, take a look at Figs. 7.12 and 7.16. The address bus isn't stable until the middle, or end, of the first clock cycle, and the address strobes (used for most memory access) aren't stable until the middle of the second clock cycle. The decision to assert DTACK* has to be made before the middle of the third clock cycle. So there is really only one clock cycle for data access.

2) For 8 bit I/O devices, there seems to be a wide variety of ways the 8 bit I/O devices is connected to the data lines. A lot of them seem to use the upper most byte on the data bus. The TS2 puts one 6850 on the high byte and the other 6850 on the low byte. Why do most people use the high data bus byte for accessing 8 bit devices?

I don't think there is any actual technical reason to choose the high or low data byte for 8-bit access. Maybe just convenience? One would require using even addresses, the other, odd addresses (for the 8-bit device). MOVEP can be used for 8-bit devices, and I don't believe there is any advantage for either even or odd addresses.

Roger