Subject: Re: Gryphon 68030
Posted by yoda on Thu, 09 Mar 2017 19:50:04 GMT
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lynchaj wrote on Thu, 09 March 2017 09:52Hi

The Jackalope board supports UART TTL headers for USB converter cables already and the legacy RS-232 ports for those going old-school. For those who don't like one or the other just leave those pads unpopulated as it won't matter.

Yes, there has been a lot of movement on the DRAM controllers of late. Apparently work continues on the KISS-68030 and there may be a new and improved version of the DRAM controller by the time we're ready for step two. The Tobster DRAM controller might be an option too so we'll just have to see what's the best way forward once we get there.

The good news is Jackalope is basically ready for production now. All the designs have been updated, the PCB trace routed and optimized. All it needs is an order and we'll have much improved next generation boards -- regardless of the merits of the design.

The Gryphon project is still a long ways from done though. To realistically run Linux it has to have more CPU throughput and DRAM capacity which are addressed in the plan posted above.

well if you would commit to UART TTL then you could bring the headers for it closer to board edge and support right angle connector which would be a little more flexible.

There is no reason for some of the things suggested not to happen in parallel instead of serially. I still sense you leaning towards an 030 as an end game vs a 040 design. The goal of Alderaan is to get a CPLD DRAM controller with known working base I/O. That is why it is not a rich I/O system - the focus is on memory and test out the 68150 which is essentially required to get an 040 to work. I don't believe in changing a lot at once. The board will have 2MB of SRAM on it which will allow a good monitor to be developed and test out the DRAM. The serial, parallel ports and IDE are already known to work so there is less to debug.

So who is going to order and distribute the Jackalope board. And also who is actively going to help bring up the board and flesh out the design? There is more logic that can probably be subsumed by the CPLD once it is working. I am imagining the wait state generators will fit and possibly the byte decode logic.

Dave