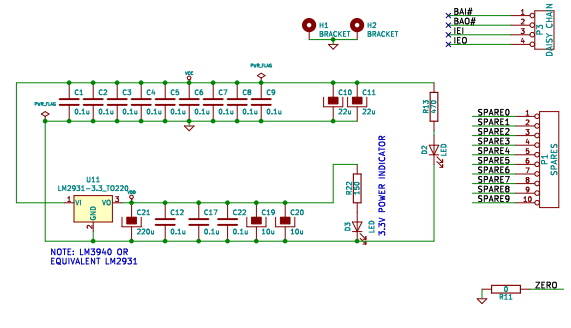
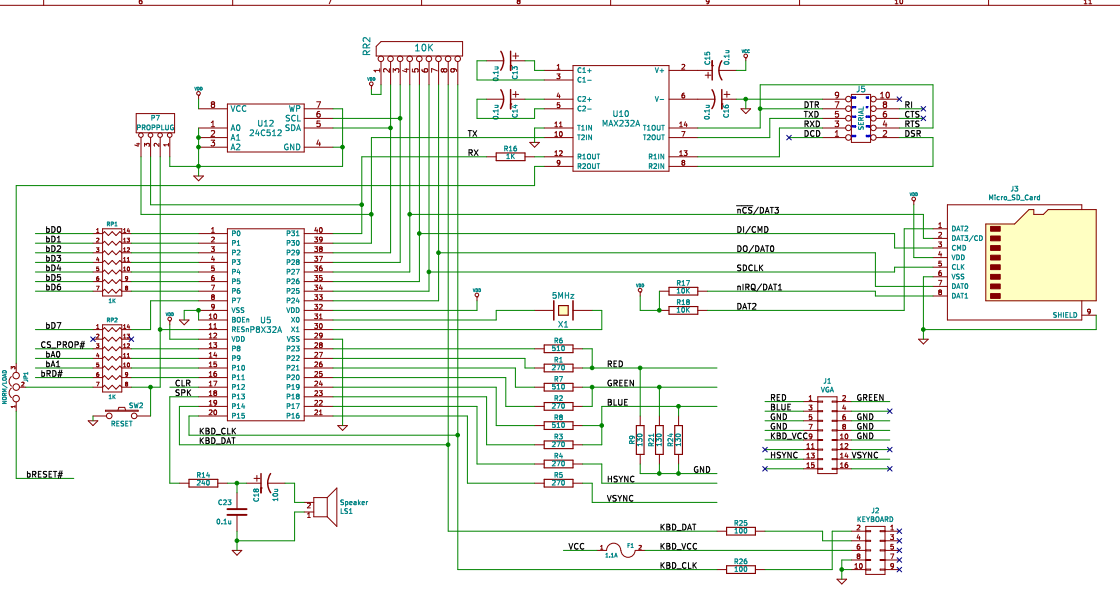


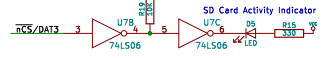
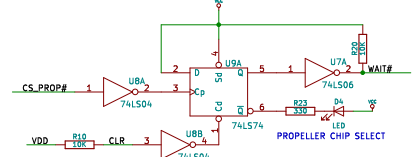
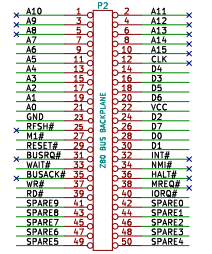
Note: IO Address Ports S#B-S#B  
 S1=off - A7 (high)  
 S2=on - A6 (low)  
 S3=off - A5 (high)  
 S4=on - A4 (low)  
 S5=off - A3 (high)  
 S6=on - A2 (low)  
 S7=x - A1 (no effect)  
 S8=x - A0 (no effect)

Note: Inhibit Board Operation During Interrupts  
 M1# = low, IORQ# = low

Note: Buffers and Transceivers respond to IO and MEM cycles



Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.



Spare Components

