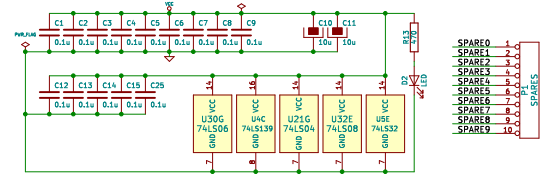


Note: Buffers/transceivers respond to IO and MEM cycles

Note: Inhibit Board Operation During Interrupts
 MIF = low, IOREQ# = low



Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.

*A10	1	2	A11	*
*A9	3	4	A12	*
*A8	5	6	A13	*
*A7	7	8	A14	*
*A6	9	10	A15	*
*A5	11	12	CLR	*
*A4	13	14	D4	*
*A3	15	16	D3	*
*A2	17	18	D2	*
*A1	19	20	D1	*
*A0	21	22	VCC	*
GND	23	24	D0	*
*RFSH#	25	26	D7	*
*MIF	27	28	DD	*
*RESET#	29	30	D1	*
*BUSRQ#	31	32	INT#	*
*WAIT#	33	34	NMI#	*
*BUSACK#	35	36	HALT#	*
*WR#	37	38	MREQ#	*
*RD#	39	40	IOREQ#	*
SPARE9	41	42	SPARE0	*
SPARE8	43	44	SPARE1	*
SPARE7	45	46	SPARE2	*
SPARE6	47	48	SPARE3	*
SPARE5	49	50	SPARE4	*

