Z80 BUS INTERFACE

IO SELECTION CIRCUIT

IO PORT ADDR

SET IO PORT

Note: IO Address Port $B8-BF
S1=off - A7 (high)
S2=on - A6 (low)
S3=off - A5 (high)
S4=off - A4 (high)
S5=off - A3 (high)
S6=x - A2 (no effect)
S7=x - A1 (no effect)
S8=x - A0 (no effect)

Note: Buffers and Transceivers respond to IO and MEM cycles

Note: Inhibit Board Operation During Interrupts
M1# = low, IORQ# = low, IA = low

Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.

Spare Components

GND PIN 11
VCC PIN 26

NOTE: U13B OC AND GATE WAS 74LS08 IN ORIGINAL

IA: HIGH DURING INTERRUPT ACTIVE
LOW DURING NORMAL OPERATION

NOTE: INT# AND NMI# RELY ON 4700 OHM PULL UP ON PROCESSOR

Sheet: /		
File: Z80DUALPIO.sch		
Title:		
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.10)-1		Id: 1/1