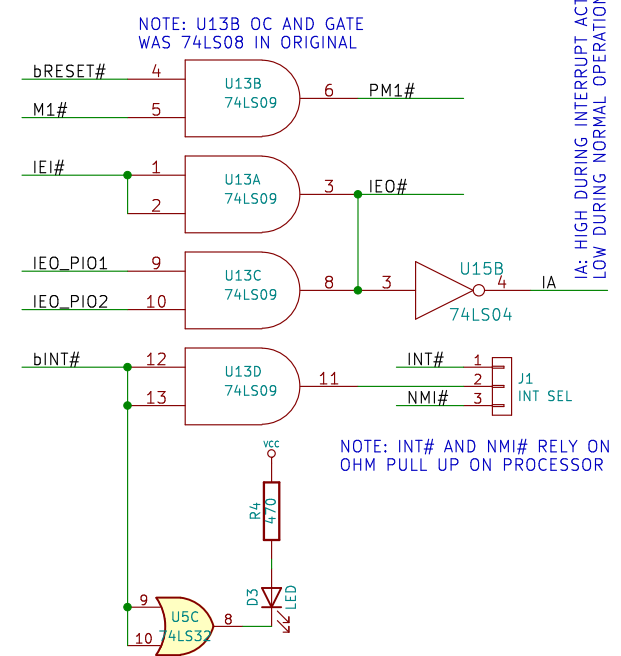
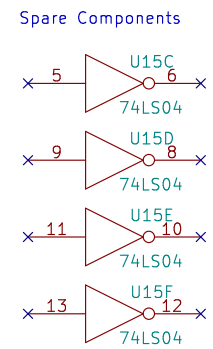
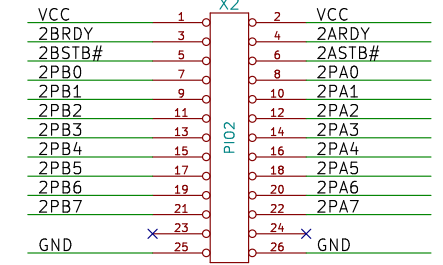
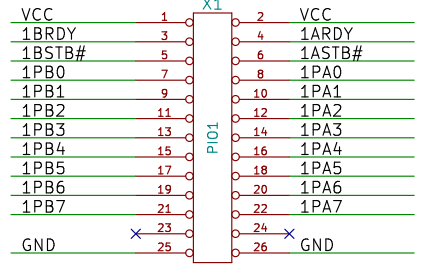
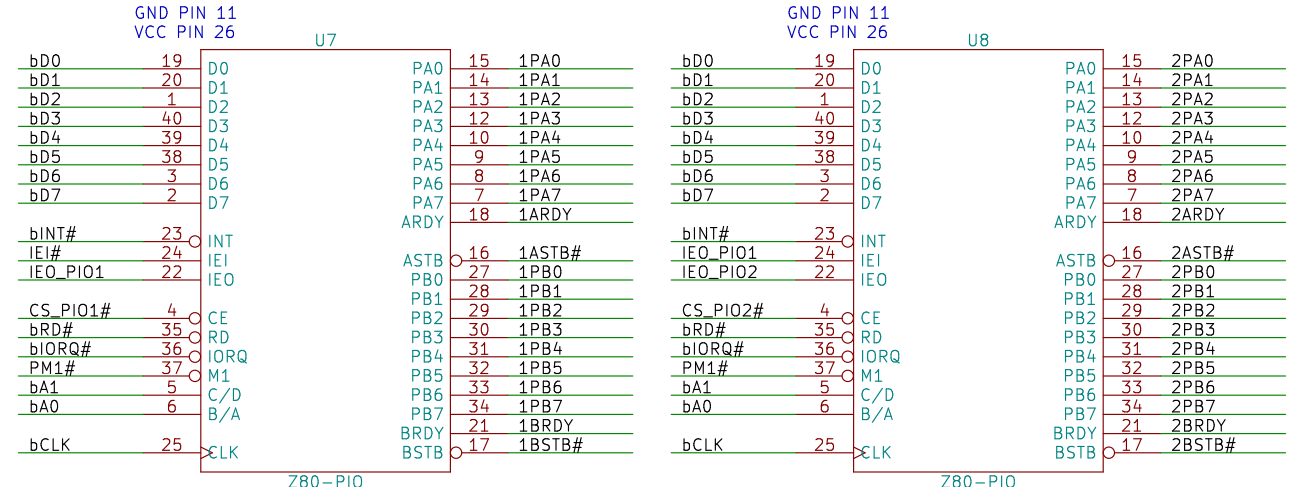
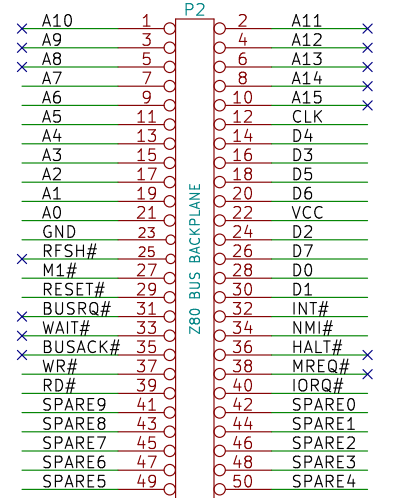


Note: Buffers and Transceivers respond to IO and MEM cycles

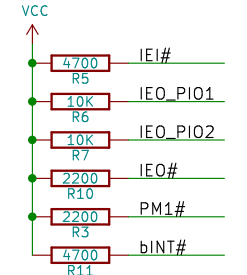
Note: Inhibit Board Operation During Interrupts  
M1# = low, IORQ# = low, IA = low

Note: IO Address Port \$B8-BF  
S1=off - A7 (high)  
S2=on - A6 (low)  
S3=off - A5 (high)  
S4=off - A4 (high)  
S5=off - A3 (high)  
S6=x - A2 (no effect)  
S7=x - A1 (no effect)  
S8=x - A0 (no effect)

Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.



NOTE: INT# AND NMI# RELY ON 470 OHM PULL UP ON PROCESSOR



NOTE: U13B OC AND GATE WAS 74LS08 IN ORIGINAL

