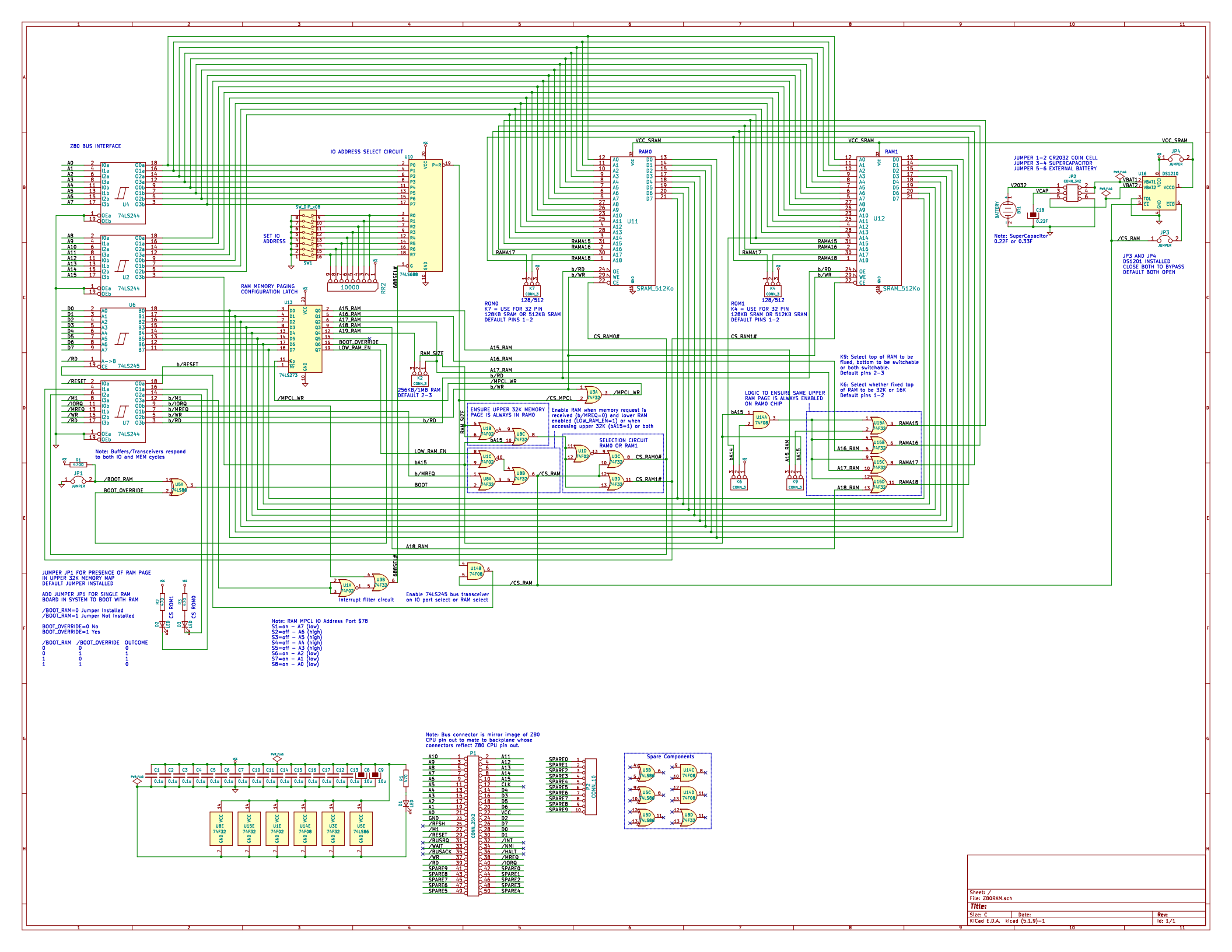
Z80 BUS INTERFACE
IO ADDRESS SELECT CIRCUIT
SET IO ADDRESS
RAM MEMORY PAGING CONFIGURATION LATCH
ROM0
K7 = USE FOR 32 PIN 128KB SRAM OR 512KB SRAM DEFAULT PINS 1–2
ROM1
K4 = USE FOR 32 PIN 128KB SRAM OR 512KB SRAM DEFAULT PINS 1–2
256KB/1MB RAM DEFAULT 2–3
ENSURE UPPER 32K MEMORY PAGE IS ALWAYS IN RAM0
Enable RAM when memory request is received (b/MREQ=0) and lower RAM enabled (LOW_RAM_EN=1) or when accessing upper 32K (bA15=1) or both
SELECTION CIRCUIT RAM0 OR RAM1
LOGIC TO ENSURE SAME UPPER RAM PAGE IS ALWAYS ENABLED ON RAM0 CHIP
K9: Select top of RAM to be fixed, bottom to be switchable or both switchable. Default pins 2–3
K6: Select whether fixed top of RAM to be 32K or 16K Default pins 1–2
JUMPER 1–2 CR2032 COIN CELL
JUMPER 3–4 SUPERCAPACITOR
JUMPER 5–6 EXTERNAL BATTERY
Note: SuperCapacitor 0.22F or 0.33F
JP3 AND JP4 DS1201 INSTALLED
CLOSE BOTH TO BYPASS
DEFAULT BOTH OPEN
Note: Buffers/Transceivers respond to both IO and MEM cycles
JUMPER JP1 FOR PRESENCE OF RAM PAGE IN UPPER 32K MEMORY MAP
DEFAULT JUMPER INSTALLED
ADD JUMPER JP1 FOR SINGLE RAM BOARD IN SYSTEM TO BOOT WITH RAM
/BOOT_RAM=0 Jumper Installed
/BOOT_RAM=1 Jumper Not Installed
BOOT_OVERRIDE=0 No
BOOT_OVERRIDE=1 Yes
/BOOT_RAM /BOOT_OVERRIDE OUTCOME
0 0 0
0 1 1
1 0 1
1 1 0
Interrupt filter circuit
Enable 74LS245 bus transceiver on IO port select or RAM select
Note: RAM MPCL IO Address Port $78
S1=on – A7 (low)
S2=off – A6 (high)
S3=off – A5 (high)
S4=off – A4 (high)
S5=off – A3 (high)
S6=on – A2 (low)
S7=on – A1 (low)
S8=on – A0 (low)
Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.
Spare Components
Sheet: /
File: Z80RAM.sch
Title:
Size: C
Date:
Rev:
KiCad E.D.A. kicad (5.1.9)-1
Id: 1/1