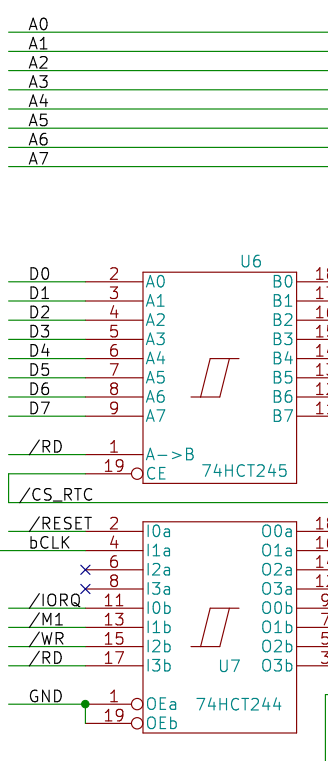
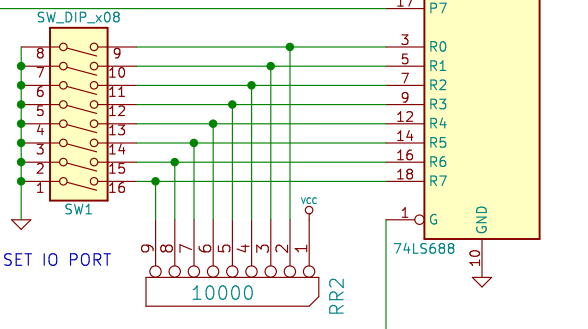


**Z80 BUS INTERFACE**



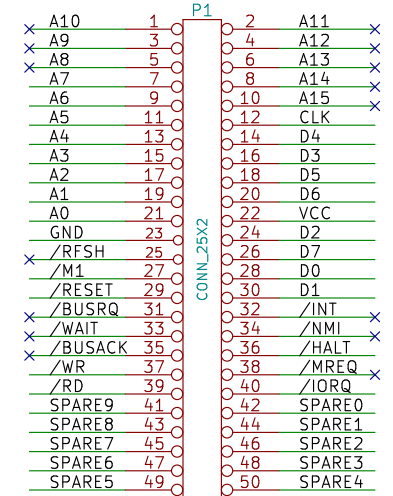
**IO SELECTION CIRCUIT**



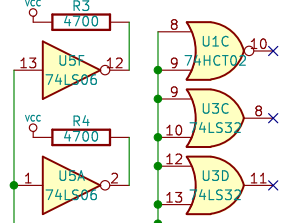
Note: IO Address Port \$70 only  
 S1=on - A7 (low)  
 S2=off - A6 (high)  
 S3=off - A5 (high)  
 S4=off - A4 (high)  
 S5=on - A3 (low)  
 S6=on - A2 (low)  
 S7=on - A1 (low)  
 S8=on - A0 (low)

Note: Inhibit Board Operation During Interrupts  
 /M1 = low, /IORD = low

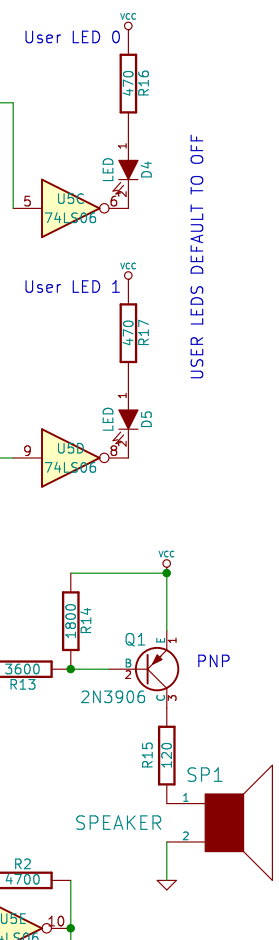
Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.



**Spare Components**



**BOARD OUTPUTS**



USER LEDS DEFAULT TO OFF

**CPU Clock Circuit**

Note: Z80 Slow Mode circuit defaults to 50% speed until CLKSEL enabled then runs at 100% CPU clock speed

Note: Accepts TTL Oscillators DIP-8 or DIP-14

JP3 installed: Slow Mode (50% or 100% clock)  
 JP3 not installed: CPU clock oscillator (default)