Microchip

SP0256B

NARRATOR™ SPEECH PROCESSOR

FEATURES

- Natural Speech
- Stand Alone Operation with Inexpensive Support Components
- Wide Operating Voltage
- Word, Phrase or Sentence Library, ROM Expandable
- Directly Expandable to a Total of 480K ROM
- Simple Interface to Most Microcomputers or Microprocessors
- Supports L.P.C. Synthesis; Formant Synthesis; and Allophone Synthesis

APPLICATIONS

- Telecommunications
- Appliances
- Computer Peripherals
- Automotive
- Personal Computers
- Toys/Games
- Educational Aids
- Warning Systems
- Security Systems
- Electronic Musical Instruments
- Aids to the Blind
- Narrow Bandwidth Communication Systems

DESCRIPTION

The SP0256B Speech Processor (SP) is a single chip N-Channel silicon gate MOS LSI device that is able, using its stored program, to synthesize speech or complex sounds.

The achievable output is equivalent to a flat frequency response ranging from 0 to 5kHz, a dynamic range of 42 dB, and a signal to noise ratio of approximately 35dB.

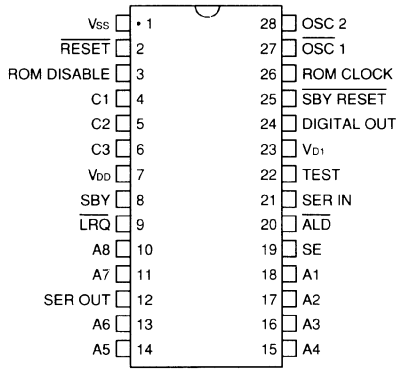
The SP0256B incorporates four basic functions:

- A software programmable digital filter that can be made to model a VOCAL TRACT.
- A 16K ROM which stores both data and instructions.
- A MICROCONTROLLER which controls the data flow from the ROM to the digital filter.
- A PULSE WIDTH MODULATOR that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

PIN CONFIGURATION

28 LEAD DUAL INLINE

Top View



ALLOPHONE BASED SPEECH PROCESSOR - SP0256AL2

One example of a preprogrammed SP0256B is the AL2 pattern.

The SP0256AL2 is available preprogrammed with a standard ROM Pattern containing 64 allophones. Through the concatenation of selected allophones the user can construct any word in the English language, thereby providing an unlimited vocabulary.

A complete description of the SP0256AL2 is contained in the SP0256AL2 Data Sheet.

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OPERATION

The addressing of the SP0256B is controlled by the address pins (A1-A8). Address Load ($\overline{ALD}$), and Strobe Enable (SE). Speech data for the SP0256B may be stored within the internal 16K ROM and/or an external serial speech ROM.

There are two modes available for loading an address into the chip. Strobe Enable (SE) controls which mode will be used.

Mode 0 (SE=0). The speech processor will latch an address when any one (or more) address pin makes a low to high transition. All address lines must be returned to the low state prior to entering a new address. (Note: Address zero (0000 0000) is not a valid address in this mode of operation.) In order to best utilize this mode of operation, a vocabulary should consist of no more than eight individual words or phrases such that single address line transitions can be made. These words or phrases must be stored using the following entry point address: 1, 2, 4, 8, 16, 32, 64 and 128.

NOTE: There is a 2 byte overhead penalty paid for each dummy entry point between the entry points actually used.

Mode 1 (SE=1). The SP0256B will latch an address using the $\overline{ALD}$ pin. The desired address is set up on the address bus (A_1-A_8) and then $\overline{ALD}$ is pulsed low. Any address can be loaded using this mode, but certain set up and hold times are required (refer to the timing diagrams for the specific times).

Two microprocessor interface pins are available for loading of addresses using mode 1. They are $\overline{LRQ}$ and SBY. Load Request ($\overline{LRQ}$) tells the processor when the address input buffer is full. Standby (SBY) tells the processor that the chip has stopped talking and no new address has been loaded. When $\overline{LRQ}$ is low, a new address may be loaded onto the address bus. Strobing $\overline{ALD}$ will cause the new address to be loaded and $\overline{LRQ}$ to go high. $\overline{LRQ}$ will return low when the address buffer is available to accept a new address. The SP0256B is capable of latching one new address while speaking the last utterance (word or phrase). The time between address load requests is variable, depending on the length of the utterance currently being spoken.

Standby (SBY) goes low when an address is loaded and will stay low until all internal instructions have been completed (i.e. the speech chip stops talking). If a second address has been loaded before the chip stops speaking the first utterance, SBY will stay low through the completion of the second utterance (ad infinitum).

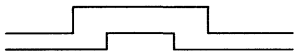
The SP0256B may be partially powered down when SBY is high to conserve battery life, provided V_{D1} remains powered. During power down and power up, reset should be held low to ensure the proper reset condition. While the speech processor is in the partial power down state, the handshake control signals ($\overline{ALD}$, SE, $\overline{LRQ}$, and SBY) and the address bus are active. However, the SP0256B will not output the addressed speech data until after V_{DD} is reapplied.

TEST MODES

The TEST pin (22) should be kept grounded at all times to avoid entering any test mode accidentally.

The test modes are entered by making TEST and one of the following pins high simultaneously; A_1, A_2, A_3 or A_5. The test pin should be made high totally within the appropriate A input. Two or more test modes may be entered together except T_0 and T_1. Pulsing RESET with TEST = 0 cancels all test modes.

A_1, A_2, A_3 and/or A_5 TEST



The following is a list of test modes:

T_0 = T. ($A_1 = A_2 = A_3 = A_5 = 0$)
T_S = T. A_1
T_2 = T. A_2
T_3 = T. A_3
T_5 = T. A_5

T_0 causes the SP0256B to ignore its internal ROM. Instructions must be supplied serially through pin 21 (serial Data In). The chip should be interfaced to an SPR000 to fully utilize this mode.

T_1 causes the SP0256B to read out its internal ROM on the Serial Address Out pin 12.

T_2 causes the internal serial data bit stream to appear on pin 24 in place of the normal DIGITAL OUT.

T_3 is used with T_2. It causes the internal coefficient data ROM to be read out if the inputs to pin 21 are appropriate.

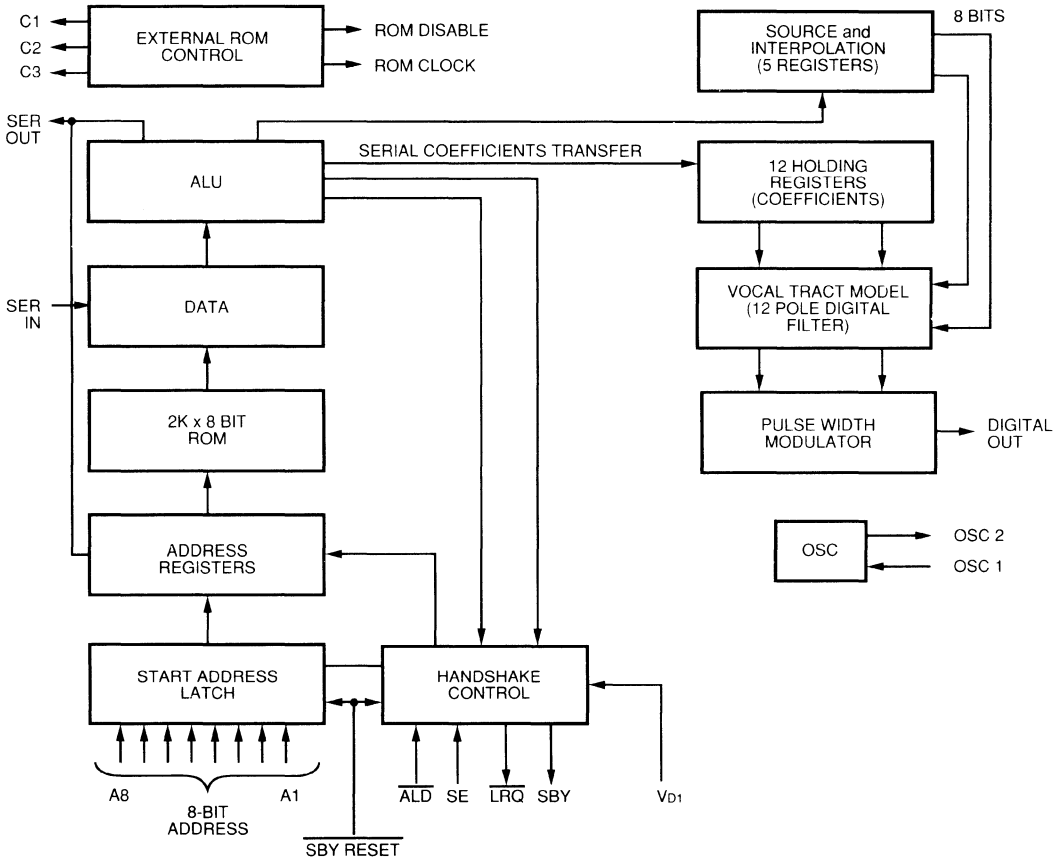
T_5 causes the internal CE (chip enable) signal to come out on pin 9 ($\overline{LRQ}$)

SPECIAL T_0 ENTRY

T_0 may be entered by wiring TEST to a permanent high and pulsing $\overline{RESET}$. T_0 will be entered and all other test modes permanently locked out. The voltage levels on any Address input is irrelevant when T_0 is entered this way.

Returning TEST to 0 will not rescind this method of entering T_0 unless $\overline{RESET}$ is pulsed.

SP0256B BLOCK DIAGRAM



PIN FUNCTIONS

Pin Number	Name	Function
1	V_{SS}	Ground
2 (input)	$\overline{RESET}$	A logic 0 resets that portion of the SP powered by V_{DD}. Must be returned to logic 1 for normal operation. Upon reset C1, C2, C3, and SBY = 1.
3 (input)	ROM DISABLE	For use with an external serial speech ROM, a logic 1 disables the external ROM.
4, 5, 6 (outputs)	C1, C2, C3	Output control lines for use with an external serial speech ROM. Refer to the SPR128A data sheet for details.
7	V_{DD}	Power supply for all portions of the SP except the microprocessor interface logic.
8 (output)	SBY	STANDBY. A logic 1 output indicates that the SP is inactive and V_{DD} can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0.
9 (output)	$\overline{LRQ}$	LOAD REQUEST. $\overline{LRQ}$ is a logic 1 output whenever the input buffer is full. When $\overline{LRQ}$ goes to a logic 0, the input port may be loaded by placing the 8 address bits on A_1-A_8 and pulsing the $\overline{ALD}$ input.
10, 11, 13, 14, 15, 16, 17, 18	A_8, A_7, A_6, A_5 A_4, A_3, A_2, A_1	8 bit address which defines any one of 256 speech entry points.
12 (output)	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM. When $\overline{RESET}$ and $\overline{SBY\ RESET}$ go to 0, SER OUT goes to 1.
19 (input)	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, $\overline{ALD}$ is disabled and the SP will automatically latch in the address on the input bus approximately 1us after detecting a logic 1 on any address line.
20 (input)	$\overline{ALD}$	$\overline{ADDRESS\ LOAD}$. A negatiave pulse on this input loads the 8 address bits into the input port. The negative edge of this pulse causes $\overline{LRQ}$ to go high.
21 (input)	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22 (input)	TEST	This pin should be grounded for normal operation. A logic 1 places the SP0256B in its test mode.

PIN FUNCTIONS

Pin Number	Name	Function
23	V_{D1}	Power supply for the microprocessor interface logic and controller. When not tied to V_{DD}, V_{D1} must remain high.
24 (output)	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5kHz low pass filter and amplifier, will drive a loudspeaker.
25 (input)	$\overline{\text{SBY RESET}}$	$\overline{\text{STANDBY RESET}}$. A logic 0 resets the microprocessor interface logic and the address latches. Must be returned to logic 1 for normal operation. $\overline{\text{SBY RESET}}$ must be tied to $\overline{\text{RESET}}$ (pin 2).
26 (output)	ROM CLOCK	This is a 1.56MHz clock output used to drive an external serial speech ROM.
27 (input)	OSC1	XTAL IN. Input connection for a 3.12MHz crystal.
28 (output)	OSC2	XTAL OUT. Output connection for a 3.12MHz crystal.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All pins with respect to Vss .....-0.3V to 8.0V
Storage Temperature .....-25° C to 125° C

Standard Conditions

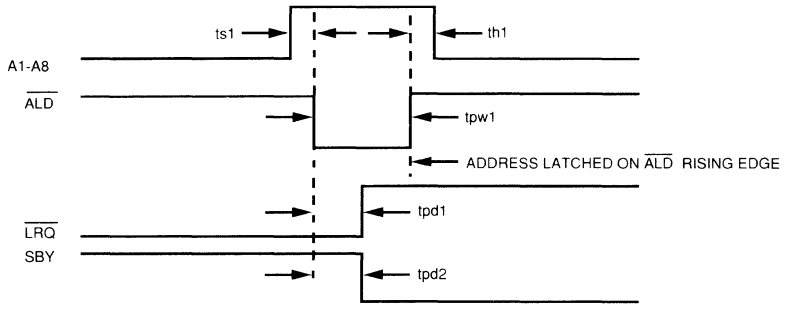
Clock - Crystal Frequency 3.120MHz
Operating Temperature .....TA = 0° C to +70° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

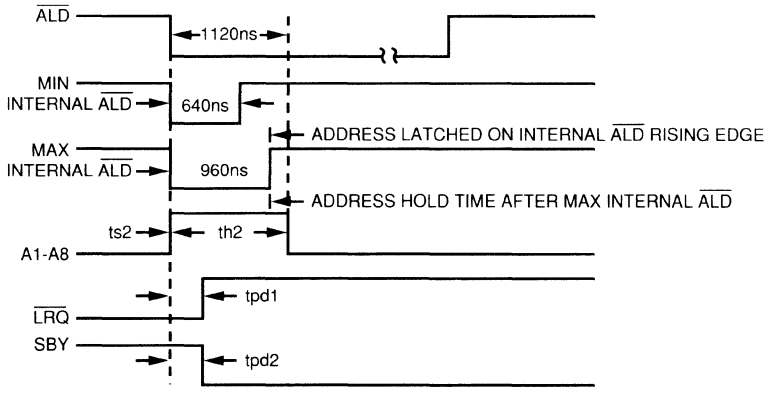
Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	VDD	4.6	-	7.0	V	
Standby Supply Voltage	VD1	4.6	-	7.0	V	
Primary Supply Current	IDD	-	80	95	mA	$\overline{\text{Reset}}$ and $\overline{\text{SBY}}$ Reset high. OSC1 = 3.12MHz. All other inputs floating.
Standby Supply Current	ID1	-	25	29	mA	Same as above.
INPUTS						
A1-A8, $\overline{\text{ALD}}$, SERIN, TEST, SE						
LOGIC 0	VIL	0.0	-	0.6	V	
LOGIC 1	VIH	2.4	-	VD1	V	
CAPACITANCE	CIN	-	-	10	pf	0 volts bias, f = 3.12 MHz
LEAKAGE	IL	-	-	10	µA	VPIN = 7.0V Other Pins = 0.0V
$\overline{\text{RESET}}$, $\overline{\text{SBY RESET}}$						
LOGIC 0	VRSIL	0.0	-	0.6	V	
LOGIC 1	VRSIH	4.0	-	VD1	V	VD1 = 4.6V
		4.6	-	VD1	V	VD1 = 7.0V
OUTPUTS						
SBY, Digital Out, C1, C2, C3, $\overline{\text{LRQ}}$, ROM DIS, ROM CLK, SEROUT						
LOGIC 0	VOL	0.0	-	0.6	V	IOL = 0.72mA (2LS TTL Loads)
LOGIC 1	VOH	2.5	-	VD1	V	IOH = -50µA (2LS TTL Loads)
OSCILLATOR						
OSC2 (Output)						When driven from ext. input
LOGIC 0	VOL	0.0	-	1.0	V	OSC1 (input) = 4.00V MIN at VD1 = 4.60V
LOGIC 1	VOH	2.5	-	VD1	V	OSC1 (input) = 0.60V MAX
Short Circuit Current on OSC2	ISC	-7.5	-	-0.4	mA	OSC1 (input) = 0.60V OSC2 (output) = 0.00V
OSC1 Input Current	IIN	-4.9	-	-0.4	µA	OSC1 (input) = 0.00V

Characteristics - AC	Sym	Min	Typ	Max	Units	Conditions
$\overline{ALD}$	tpw1	200	-	960	ns	200 ≤ $\overline{ALD}$ ≤ 960ns
A1 - A8 Set Up	ts1	160	-	-	ns	
Hold	th1	160	-	-	ns	
$\overline{LRQ}$	tpd1	-	-	300	ns	
SBY	tpd2	-	-	300	ns	

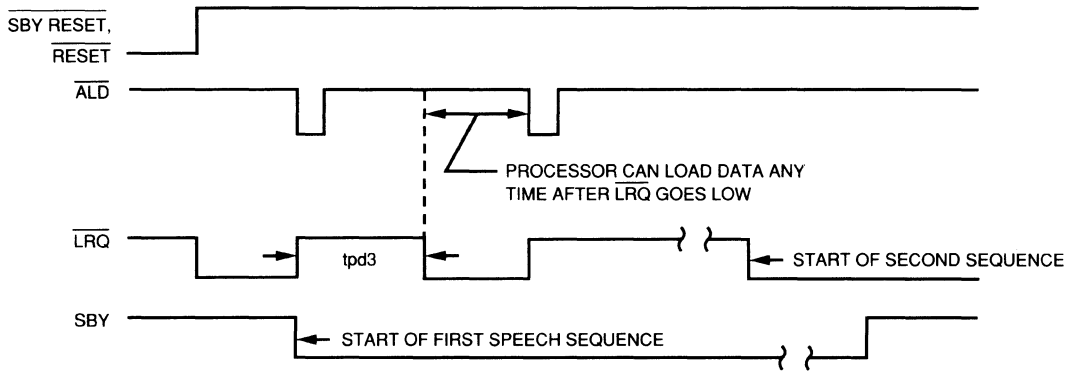


Characteristics - AC	Sym	Min	Typ	Max	Units	Conditions
A1 - A8 Set Up	ts2	0	-	-	ns	$\overline{ALD}$ > 960ns
Hold	th2	1120	-	-	ns	
$\overline{LRQ}$	tpd1	-	-	300	ns	
SBY	tpd2	-	-	300	ns	

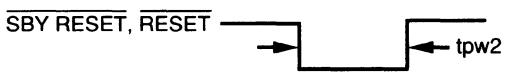


Characteristics - AC	Sym	Min	Typ	Max	Units	Conditions
$\overline{LRQ}$	tpd3	16.67	-	33.3	µs	Address Buffer ready for next load.

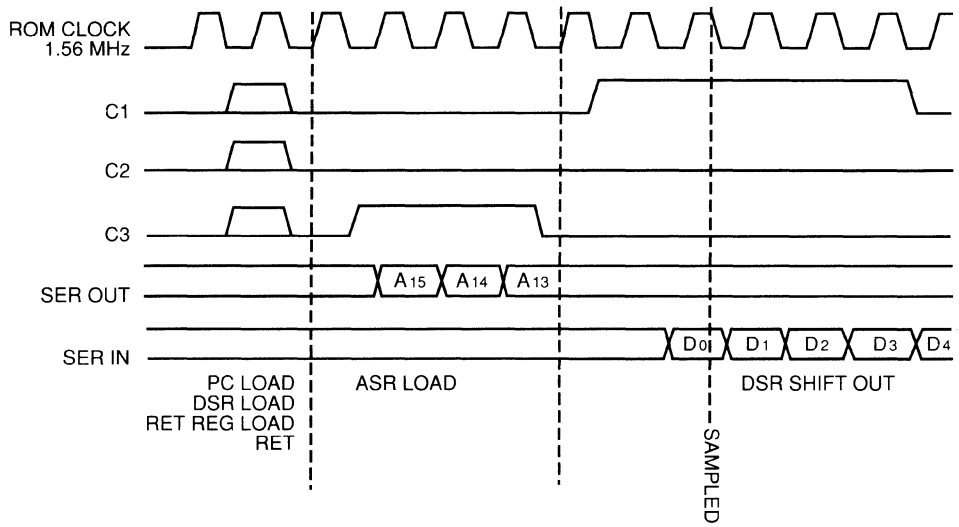
TYPICAL TIMING SEQUENCE



Characteristics - AC	Sym	Min	Typ	Max	Units	Conditions
Clock	F	-	3.120	-	MHz	Crystal oscillator driven
Clock Duty Cycle	-	48	-	52	%	from external.
Reset, SBY Reset	tpw2	25	-	-	µs	



EXTERNAL ROM INTERFACE TIMING



SPO256B EXTERNAL AND INTERNAL CONTROL LINES*

(All synchronous to the ROM clock)

C1 C2 C3

0 0 0 NOP - No Action Taken

0 0 1 ASRLD - (Address Shift Register Load) Serially shifts data (MSB first) from the serial address out pin (also occurs internally in the SP0256B into the ASR reg in preparation for loading into the PC). The ASRLD loads 16 bits of the ASR with two 8 bit load sequences followed shortly by a PCLD.

0 1 0 PCLD - Loads the contents of the ASR register into the PC. Occurs only after 16 ASRLDS have occurred.

0 1 1 DSRLD - (Data Shift Register Load) Loads the 8 bit data shift register with the contents of the ROM pointed to by the current address in the PC. The DSRLD will also shift out the LSB of the 8 bit DSR and increment the PC.

1 0 0 DSRSH - (Data Shift Register Shift) Shifts data out of DSR reg starting with the second LSB (the first LSB is shifted out with the occurrence of a DSRLD). There are seven (7) DSRSH's after every DSRLD (not necessarily consecutive).

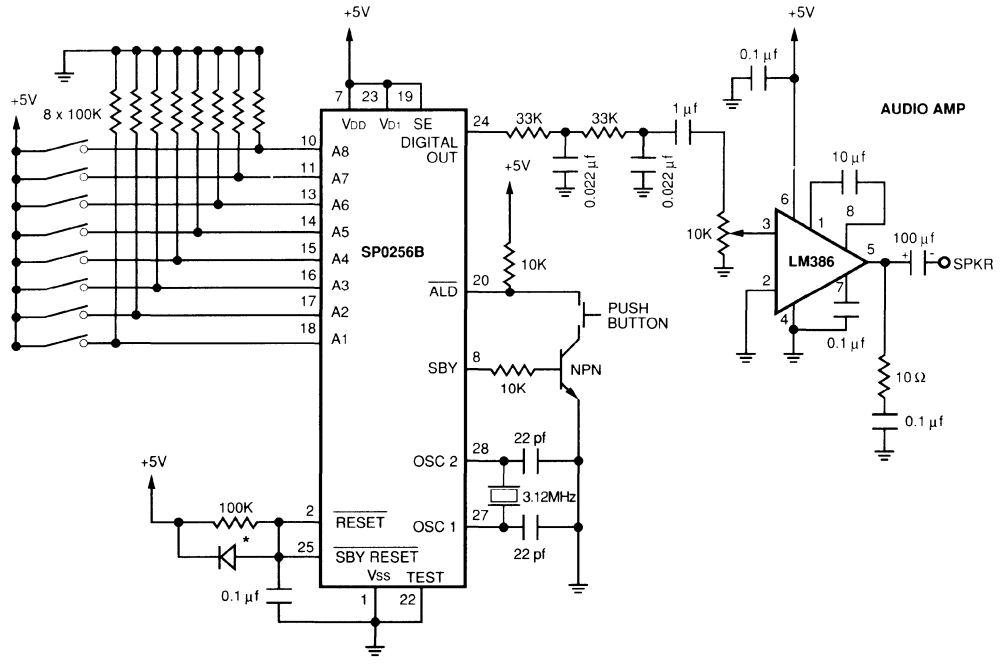
1 0 1 STACKLD - Loads the STACK with the current value of the PC.

1 1 0 RETURN - Loads the PC with the contents of the STACK.

1 1 1 Will occur in SP0256B when SBY RESET and RESET = "0".

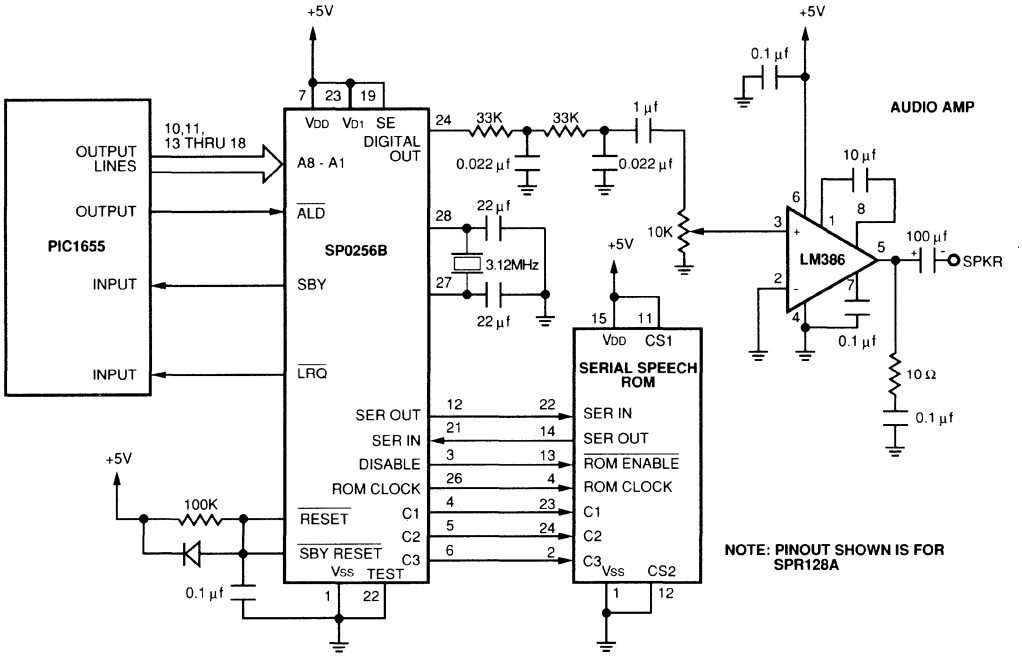
*All ROMs including the SP0256B internal ROM will be activated by the above control lines. However, only the ROM with the current chip select will be enabled to send speech data to the SP0256B.

Typical Application: Stand Alone Configuration



* Diode possibly necessary if power is turned off then on in less than 50 ms.

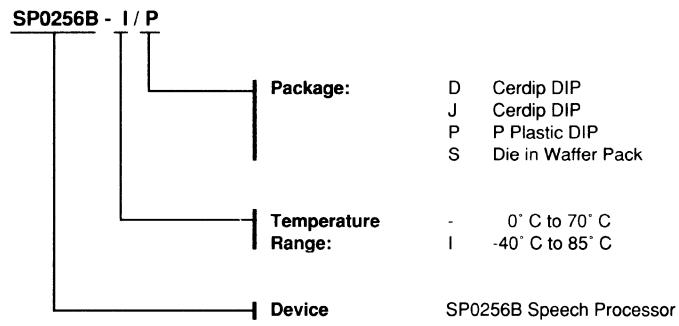
Typical Application: Microprocessor Interface



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS



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