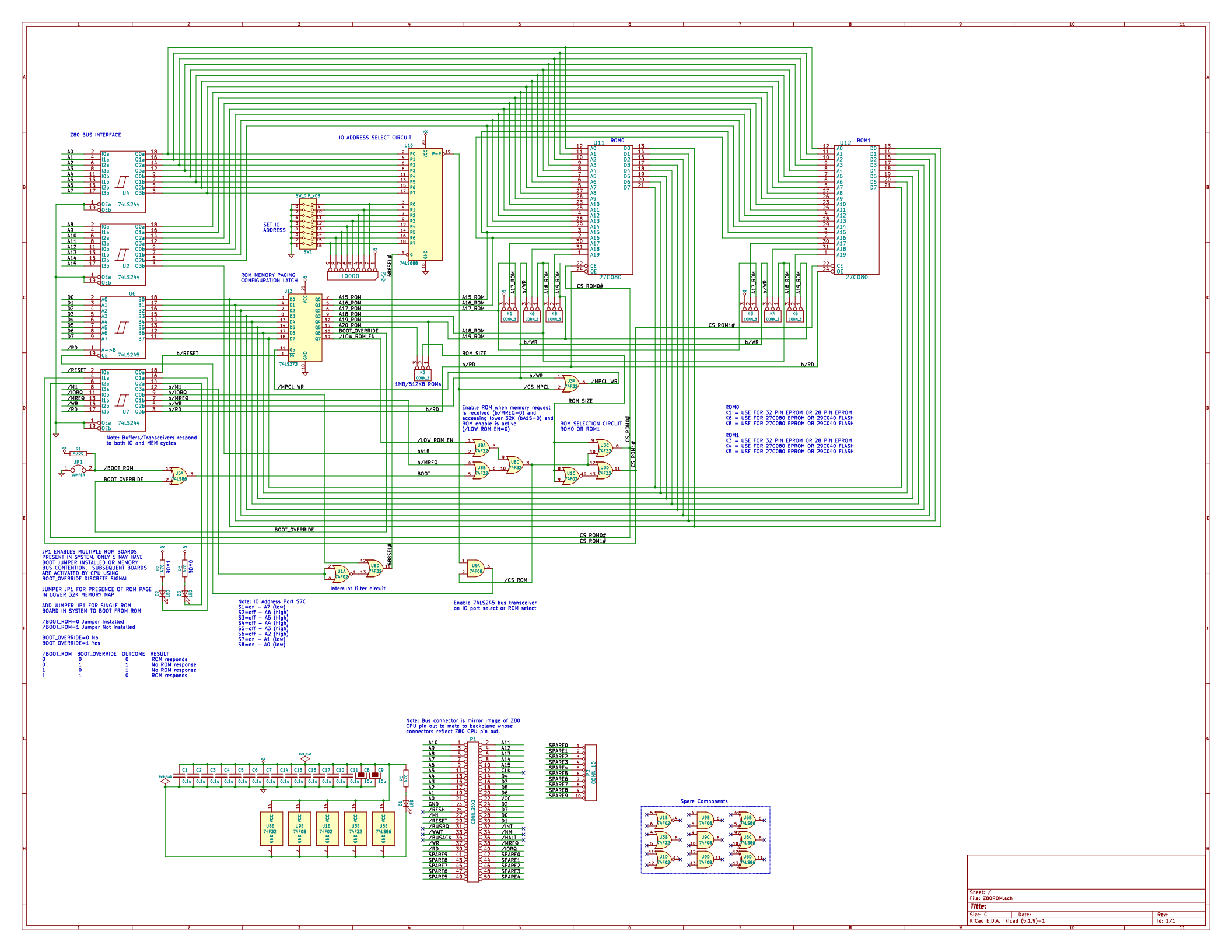
Z80 BUS INTERFACE
IO ADDRESS SELECT CIRCUIT
SET IO ADDRESS
ROM MEMORY PAGING CONFIGURATION LATCH
1MB/512KB ROMs
ROM SELECTION CIRCUIT ROM0 OR ROM1
Enable ROM when memory request is received (b/MREQ=0) and accessing lower 32K (bA15=0) and ROM enable is active (/LOW_ROM_EN=0)
Note: Buffers/Transceivers respond to both IO and MEM cycles
Interrupt filter circuit
Enable 74LS245 bus transceiver on IO port select or ROM select
ROM0
ROM1
K1 = USE FOR 32 PIN EPROM OR 28 PIN EPROM
K6 = USE FOR 27C080 EPROM OR 29C040 FLASH
K8 = USE FOR 27C080 EPROM OR 29C040 FLASH
K3 = USE FOR 32 PIN EPROM OR 28 PIN EPROM
K4 = USE FOR 27C080 EPROM OR 29C040 FLASH
K5 = USE FOR 27C080 EPROM OR 29C040 FLASH
JP1 ENABLES MULTIPLE ROM BOARDS PRESENT IN SYSTEM. ONLY 1 MAY HAVE BOOT JUMPER INSTALLED OR MEMORY BUS CONTENTION. SUBSEQUENT BOARDS ARE ACTIVATED BY CPU USING BOOT_OVERRIDE DISCRETE SIGNAL
JUMPER JP1 FOR PRESENCE OF ROM PAGE IN LOWER 32K MEMORY MAP
ADD JUMPER JP1 FOR SINGLE ROM BOARD IN SYSTEM TO BOOT FROM ROM
/BOOT_ROM=0 Jumper Installed
/BOOT_ROM=1 Jumper Not Installed
BOOT_OVERRIDE=0 No
BOOT_OVERRIDE=1 Yes
/BOOT_ROM BOOT_OVERRIDE OUTCOME RESULT
0 0 0 ROM responds
0 1 1 No ROM response
1 0 1 No ROM response
1 1 0 ROM responds
Note: IO Address Port $7C
S1=on – A7 (low)
S2=off – A6 (high)
S3=off – A5 (high)
S4=off – A4 (high)
S5=off – A3 (high)
S6=off – A2 (high)
S7=on – A1 (low)
S8=on – A0 (low)
Note: Bus connector is mirror image of Z80 CPU pin out to mate to backplane whose connectors reflect Z80 CPU pin out.
Spare Components
Sheet: /
File: Z80ROM.sch
Size: C
Date:
Rev:
KiCad E.D.A. kicad (5.1.9)-1
Id: 1/1